

ANALOG BASEBAND IC FOR USE IN DIRECT CONVERSION W-CDMA RECEIVERS

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ABSTRACT

A 0.6 μm BiCMOS Analog Baseband IC that enables a direct conversion W-CDMA receiver is described. Two diversity I/Q channels provide 87 dB of voltage gain, controllable in 1-dB steps. A 2 MHz Low Pass Filter, synchronized to an external RC network, provides an accurate rejection mechanism against adjacent channel interference. A log amp provides a "Fast-RSSI" function for rapidly selecting gain settings. Low DC current ($<5\text{mA}$ / path), low input noise ($<4\text{ nV}/\text{Hz}^{1/2}$), and a high P3dB (-20 dBVrms) are achieved.

INTRODUCTION

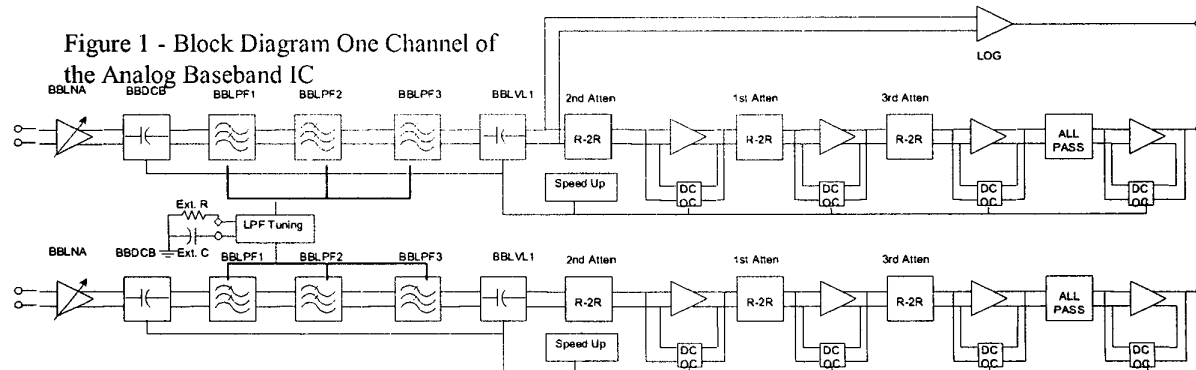
An Analog Baseband (ABB) Integrated Circuit (IC) has been developed for use in a direct conversion receiver for Wideband Code Division Multiple Access (W-CDMA). The IC contains two diversity in-phase and quadrature (IQ) receiver channels which accept baseband inputs from the RF front end and provide 2 MHz BW low pass filtered (LPF) baseband outputs to the receiver's A/D converter. Each receive I or Q channel consists of a number of specific sub-systems: Low Noise Amplifier (LNA), Low Pass Filter (LPF), and Variable Gain Amplifier (VGA). The In-phase paths of each of the two receive channels also contain a log amplifier used to determine a coarse receiver signal strength indication (RSSI) to permit rapid selection of amplifier gains. The IC is fabricated using a 0.6 μm Silicon BiCMOS process and is packaged in an FBGA.

identical IQ receive channels that are provided to allow for diversity reception. A serial interface is provided to minimize the pin count and allow the maximum flexibility in the control of the circuit. A bandgap reference circuit provides a temperature-insensitive voltage reference for all circuits.

A tuning loop synchronizes the filter cutoff frequency to an externally provided resistor and capacitor. The LNA and VGA architectures insure precise, monotonic gain control over an 87 dB system input requirement (-102dBVrms to -15 dBVrms). Care has been taken to optimize DC current consumption, inter-modulation performance, and sensitivity.

The gain control is carefully allocated between the LNA and the VGA to insure that the carrier to noise (C/N) ratio of the system improves for increasing input signal levels. This implies that the gain distribution results in neither noise limiting by introducing excessive front end attenuation, nor intermodulation / compression limiting arising from too much attenuation being placed at the output. As a result, the attenuation is first increased at the center attenuator of the VGA, then by the input attenuator and finally by the output attenuator. When the input signal has risen to a level of -44 dBVrms , further increases in input signal level cause unacceptable nonlinearity in the LPF. Above this input level, an additional 24 dB of gain can be removed at the LNA input in 6 dB steps. This allows the input level of the ABB IC to rise to as

Figure 1 shows a block diagram of one of the two



much as -30 dBVrms without gain compression; and operate properly up to -15dBVrms with amplitude compression permitted.

LNA DESIGN

The LNA consists of 16 parallel, degenerated NPN bipolar transconductance elements that have been selected to provide minimum noise figure and maximum input intercept point. Gain control is achieved by supplying DC current to a number of gain stages to achieve the desired gain. For example, a maximum voltage gain of +14 dB is provided when all 16 stages are biased simultaneously. Gain reductions of -6, -12, -18, and -24 dB are realized by supplying DC current to 8, 4, 2, and 1 stages respectively. An additional benefit of this architecture in a handset application is that the DC current is reduced as the input gain is reduced. Since this normally coincides with operation in a high signal area where the transmitter power is also reduced, the battery life of the receiver can be greatly extended in this mode. When minimum gain is selected, the DC current consumption of the LNA is reduced by a factor of five, corresponding to about 25% of the total DC current reduction.

DC BLOCK

The circuitry preceding the ABB-IC and the first LNA stage both contain first order lowpass filter sections. This provides rejection to out of band interferers, which improves the effective input IP3 of the IC. As a result, the DC current consumption can be reduced to approximately 25% of other reported implementations [1]. The output of the passive RC LPF is DC blocked using a passive RC highpass section to minimize the effect of the internal DC offsets from limiting the dynamic range of the receiver. Without the addition of DC blocking or offset correction in strategic areas of the IC, small DC offsets at the input could quickly limit the performance of a receiver chain with 86 dB of DC gain (-102 dBVrms worst case ABB-IC input noise floor at minimum signal level to -16 dBVrms output). The spread spectrum nature of W-CDMA tolerates the removal of the lowest few kHz of frequency response with insignificant systemic bit error rate (BER) degradation [2].

LOWPASS FILTER

The low pass filter (LPF) uses a repeated transconductance cell to implement a 5th order Cauer-Chebyshev (CC) response. This characteristic was carefully chosen because it provides the optimum amplitude response and group delay characteristics. The LPF begins with a gm/C integrator stage, which provides additional initial rejection at out of band

frequencies to improve the effective input IP3 of the IC. This cell is a differential stage made up of NMOS FETs whose transconductance can be adjusted through the use of an external control signal to tune the cutoff frequency of the LPF. The key to the design is the use of low-Q, LC resonators, where the inductors are synthesized using gyrators.

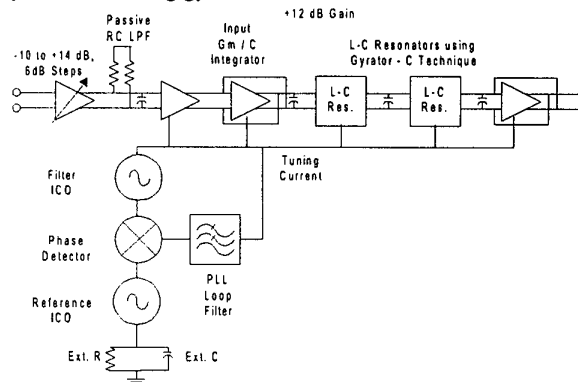


Figure 2-Simplified Block Diagram of LP Filter

The cutoff frequency is a key design consideration as it limits the adjacent channel selectivity of the system. A phase locked loop is used to insure that the effective transconductance of the filter elements is locked to external, precise (<2%) resistors and capacitors. Using this technique, extremely good absolute tolerances can be maintained. The PLL can compensate for changes in circuit parameters over variations in temperature and process. A simplified block diagram of the LPF design is shown in Figure 2. In the system, achieving the required adjacent channel selectivity (ACS) is predicated upon maintaining LPF cutoff frequency accuracy within 10% over process and temperature. This requirement also obviates the requirement to align the cutoff frequency during assembly of the product resulting in cost savings.

VARIABLE GAIN AMPLIFIER

The design considerations of the VGA are dominated by the need for precise control of the gain characteristic versus desired gain level. The approach selected employs a set of voltage amplifiers that alternate with a set of precision attenuators. The VGA input is supplied by the output of a level shifter. This signal is applied to the first attenuator. The attenuator uses a balanced R-2R ladder to provide precision control of the attenuation. Since all of the resistors in the R-2R ladder are ratiometric, variations due to process or temperature have minimal impact on the attenuation characteristic. In this implementation, arrays of nMOS FETs act as switches to select the

appropriate rung of the balanced R-2R ladder. An additional advantage of this design approach is that the input impedance of the ladder is independent of the attenuation state selected. This minimizes gain variations due to the finite source impedance driving the attenuator input.

Each of the three R-2R ladders consist of five 6dB sections for 30 dB of gain control per ladder or a total of 90 dB of gain control in 6.02 dB steps total. To achieve the 1 dB steps, the feedback resistance of the op amps can be switched using NMOS FETs to provide 1, 2, and 4 dB of additional gain reduction. In total, the VGA is capable of providing monotonic gain control in 1dB steps over a 95 dB range. An additional responsibility of the VGA is to compensate for gain variations in the RF front end components, and the ABB-IC itself. This imposes a requirement for an additional 10 dB of additional gain control on top of the nominal 82 dB system requirement (-98dBVrms nominal input to -16 dBVrms output) yielding a requirement of 92 dB. Between the third and fourth opamp stages, an all-pass network has been added to correct the overall group delay. Careful layout of the IC resulted in achieving this range without instability or oscillation.

RECEIVED SIGNAL STRENGTH INDICATOR

The inphase channel of each receive path contains a log amp to allow a "fast RSSI" function to be implemented. The log amp consists of a cascade of five detector cells with 4 amplifier cells in between them. The five detectors are summed to achieve a proportionality constant of approximately 25 mV/dB over a 70dB dynamic range. This function was achieved with the exceptionally low DC current of less than 300 uA.

ANCILLARY FUNCTIONS

The three wire (Enable, Data, and Clock) serial interface provides control with a minimum number of interface lines. The serial port is entirely CMOS and draws no DC current as long as the clock receives no input. To further minimize unnecessary DC current consumption, several reduced power "sleep" modes are implemented. These modes are implemented asynchronously through external pins to allow sleep modes to be selected for the maximum amount of time. Each channel can be put in sleep mode independently. The requirement of a very low cutoff frequency for the highpass circuit presents a difficult problem in a circuit that is to be frequently powered down to save DC current. In the event that the circuit is powered up, or the sleep mode is changed, or in certain other

circumstances, a transient impulse can propagate through the receive chain. This will have the effect of saturating the receiver until such time as the transient dies out. Since the cutoff frequency of the HPF is ~ 5 KHz, it will take several time constants of $1 / (5 \times 10^3)$ seconds to recover. To avoid this lengthy, dc current consuming condition, a speedup circuit is included. The speedup circuit increases the cutoff frequency of the highpass circuits for a very short time to allow the capacitors to rapidly charge or discharge to the desired value. Once the transient has decayed, the speedup circuit is turned off to provide the full operational bandwidth for the circuit.

SYSTEM PERFORMANCE

The performance of the ABB-IC in a system is shown in Figure 3. Less than +/- .6dB of integrated non-linearity is observed over the worst case system required linear range of 72 dB from -102 dBV to -30 dBV. Operation to -15dBV is achieved with up to 7dB amplitude compression, which still permits system operation without degraded BER. Over the full operating range, differential non-linearity is less than +/- .3 dB over -102 to -15 dBVrms. DC current is 20 mA with both receive paths on; 12 mA for single path.

Figure 4 compares the RSSI output of the complete ABB-IC (lower curve) to the output of a logamp test circuit driven by an external generator without an attenuator (upper curve). Under nominal conditions, 57 dB of the logamp's dynamic range will be used from -102 dBVrms, where the output is noise limited, to -45 dBVrms, the upper limit of the LPF's linear output.

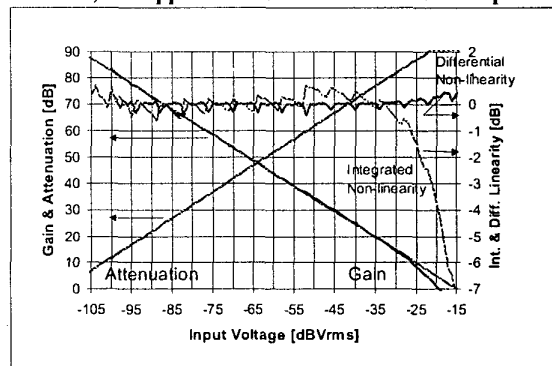


Figure 3 - Gain and Linearity of One Channel of the ABB-IC

Above this level, 6 dB of attenuation is added at the LNA for every doubling of the input voltage, which results in the resulting sawtooth voltage at the output of the RSSI thus extending the range of the system. To account for variations in the RF gain preceding the

logamp, a minimum of 65 dB of dynamic range is required in the logamp. The upper curve demonstrates that the logamp is capable of more than 70 dB range. In the receiver, the RSSI output is used to determine an approximate setting for the gain of the VGA that follows the LPF. The system requirement for RSSI precision is ± 3 dB; the measured RSSI error is 1.3dB worst case.

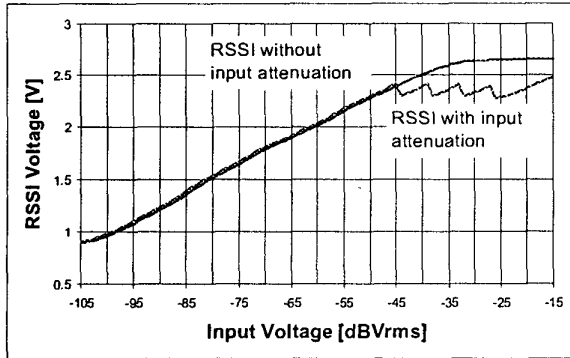


Figure 4 - RSSI Output vs. Input Voltage

CONCLUSIONS

An analog baseband IC, shown in Figure 5, has been presented which, combined with an RF front end [3], enables a 3-G Direct Conversion W-CDMA receiver at a fraction of the DC current necessary, and with a significant reduction in the number of components, to implement the receiver using a heterodyne technique. The use of inexpensive passive components to set the LPF cutoff frequency, and the DC offset compensation scheme are novel techniques which permit the cost of the receiver to be minimized. These innovations have been applied to both Mobile and Base Station 3-G cellular applications [4].

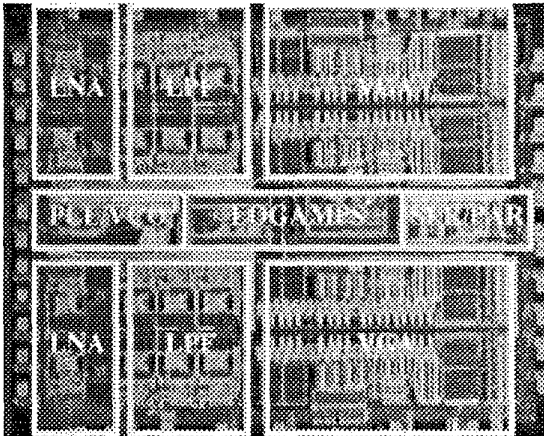


Figure 5 Micrograph of Analog Baseband IC Die

Performance Specification	System Requirement	IC Performance
Input Linear Range[dBVrms]	-102 to -30	-102 to -26
Input Total Range[dBVrms]	-102 to -15	-102 to -15
Input Noise Density [nV/11z^.5]	< 4.5	4.0
DC Current [mA]	minimum	20,dual IQ ch 12,single IQ ch
Integral Non-linearity [dB]	< 1.0	0.6
Differential Non-linearity [dB]	<0.5	0.3
RSSI Precision[dB]	< 3.0	< 1.3
Effective 11P3 [dBm]	> -24	> -22

Table 1 – IC Performance vs. System Requirements

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