

Analog at Milepost 2000: A Personal Perspective

BARRIE GILBERT, FELLOW, IEEE

Invited Paper

Electronics has barely just begun to exploit the endless opportunities for analog techniques. Rather than rendering them obsolete, the recent explosion in digital communications systems has only increased the demand for both fully analog and mixed-signal integrated-circuit (IC) products. This paper is an unashamedly personal and bipolar-centric review of a few selected aspects of the contemporary landscape and offers several reasons for expecting an unending dependence on analog techniques.

Keywords—Analog design, BJT technologies, physical circuits.

Some years ago, those of us skilled in the analog arts were on the defensive. Young zealots from the dark side—inculcated during their college days in the unequivocal laws of ones and zeros, shunning volts and amps, and with the recently invented microprocessor warm in their back pockets—were invading our time-honored domain. They were exploiting *digital techniques* to achieve all manner of functions once safely and securely out of their reach.

The threat of the decline of all things analog was never more apparent than during a visit I made to the Science Museum in London in 1982. Wandering around halls devoted to the history of computing, I found a display marked “*Obsolete Techniques*.” Alongside a nostalgic assortment of relay boards, vacuum-tube operational amplifiers, patch panels, and electromechanical servo systems was a monolithic analog multiplier I had designed in the early 1970s. At first I was surprised, then embarrassed, and soon irritated at the curators. “What do *they* know?” I fumed. Although the implication stung a little, I later took solace as I walked back into the cool evening air of South Kensington in the knowledge that this particular product not only remained firmly in the catalog, but was generating admirable revenues. It still does more than a quarter of a century since its design. *Analog is durable.*

Now that digital signal processing (DSP) has attained maturity, its dazzling successes permeate every corner of our lives. Nonetheless, that period of apprehension has passed. It

has become apparent that rather than obsoleting analog techniques, the digital era has only created endless new demands for analog circuits and demonstrated more clearly than ever before the permanence of their role as indispensable *physical* allies to the *logical* world of binary-coded representations and algorithm engines. Ultimately, the use of DSP in the manipulation of real-world signals will always be dependent on the availability of the special kind of bridging functions provided by the *analog-to-digital converter* (ADC) and *digital-to-analog converter* (DAC). While having a confused identity, these are essentially analog in terms of their design challenges, more obviously so as the sampling rates move into the hundreds of megahertz range, a domain formerly occupied only by VHF and UHF radio systems. But we are far from the time when these are the sole allies needed in the realization of modern communications systems.

Other circuit techniques, which may be called *quasi-analog* and developed in parallel to DSP during the past couple of decades, have proven astonishingly successful. These are not digital circuits, executing algorithms on coded representations of analog signals, but, nonetheless, use *binary* signals to gain their various advantages and employ cells that lay down comfortably on a digital process technology. The earliest of these was the *delta-modulator*. The idea of using a *duty cycle* D of infinite resolution over the dimensionless domain $0 > D > 1$ to represent signal samples quantized only along the time axis must have occurred to a lot of people in the course of electronic's short history. It certainly did to me and I recall developing such a modulator in 1952 using vacuum tubes, of course, and believing (incorrectly, I have no doubt) that the idea was original. More recently, sophisticated IC embodiments of the duty-cycle idea, generally known as *sigma-delta* techniques, have been devised. Duty-cycle representations of analog variables can also be found in modern high-efficiency (Class-D) audio amplifiers and certain types of sensor interfaces (such as temperature-to-duty cycle).

But these ideas had to await the sheer potency of very-large-scale integration (VLSI)—which allows thousands of digital gates (the exact number is often unknown) to be thrown at a signal-processing function—to create what

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The author is with Analog Devices Inc., Beaverton, OR 97006-1994 USA (e-mail: barrie.gilbert@analog.com).

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is essentially a new and distinct third branch of electronics, neither fully analog nor purely digital. These new ways of using low-quality cells to realize high-quality analog functions, once thought to be quite out of reach of digital sorcery, have deservedly earned our admiration. It is precisely the success of binary-intensive techniques in general, however, that has led to a popular view of the classical analog domain that is out of touch with reality. The adjective *digital*, bounteously applied to every imaginable sort of modern electronic product and service, has become all but synonymous with the notion of *fundamentally superior in every conceivable respect* compared to “old fashioned” and “outmoded” analog systems.

There is ample reason to boast about progress in modern electronics, but not *exclusively* for “being digital.” Behind every success in what are lavishly labeled digital phones, digital data systems, digital audio, digital music synthesis, digital (“*and therefore*” high-definition) television, digital cameras, digital recorders, digital copiers and fax machines, the personal digital assistant, and all manner of digitally augmented instrumentation in medicine, automobiles, and home appliances, there remains a huge supporting cast of indispensable analog components. This is easily forgotten and sometimes deliberately hidden as if the admission of the use of anything analog were an embarrassment in a world increasingly shaped by the shallow hype churned out by the image makers.¹

The undiminished demand for more capable analog circuits is especially true in that most digital of domains, the Internet, which has spawned *digital markets* and *digital commerce* based on presumptuously labeled *digital communications*. I personally feel rather offended by the deliberate obfuscation of the true nature of these communications systems, predicated on the market value of the magic word “*digital*.” The undeniably potent use of digital formats, protocols, coding, modulation, and error-correction in these grandchildren of the telephone, as marvelous as they are, can easily obscure the fact that the physical channels remain essentially and securely analog. *In the 21st century, new analog design challenges will be plentiful.*

There is ample evidence that predictions claiming analog techniques would become irrelevant to modern times were not just premature, but fundamentally lacking a foundation in common sense. At no time was there any factual basis for believing that analog circuits were ever going to be in total eclipse. Certainly, the industry did pass through a period when fundamental circuit concepts received far less emphasis than the more dazzling topic of VLSI, in many centers of learning and we are still suffering from this oversight. Even that most prestigious forum for premiering circuit innovations, the International Solid State Circuits Conference (ISSCC) showed signs of becoming a *systems* conference:

¹It is not all hype, of course. Analog circuits have a reputation for being quirky, prone to drift and loss of calibration, and to bursting into oscillation without warning. Some of this can be traced to inept design, but parametric sensitivities are unavoidable and the fight for robustness is unending. Modern system designers are prudent in seeking ways to reduce the “analog front end” to the barest minimum and often correct in declaring that “This is where all our problems are.”

many of the papers revealed no new *circuit* advances; only block diagrams. Recently, this trend appears to have somewhat slowed and even reversed as our dependence on physical channels has deepened.

Nevertheless, the diminished attention given to the crafting of analog cells, and the unwarranted, even naïve, assumption that all functions of importance will be implemented using digital techniques, had led to a shortage of skilled analog designers; only recently has the shortfall become widely recognized. Today we are witnessing something in the nature of an analog renaissance. Evidence of a renewed sensitivity to the importance of analog techniques is found in the numerous short courses in analog IC design, particularly in the RF arena. Further testimony of revitalization is provided by the many “wireless” and “communications” design centers that are popping up in favored geographical areas, offering first-rate technical challenges for people who have not forgotten Shockley’s junction equation or Ohm’s Law. (Interviews reveal that such lapses of memory are not rare.)

Design productivity is often higher at such sites, since these engineers-on-a-wire enjoy access to all the intellectual, manufacturing, and administrative resources of a large company, but without the financial risks attendant to a small startup operation, while the crucial sense of identity, mission, and the can-do spirit that characterizes and permeates a entrepreneurial endeavor are elevated. Behind the scenes, there is constant competition in seeking and hiring even marginally gifted analog designers to head up these operations. Companies offer outrageous incentives to get these people “on the team,” whether at the corporate site or in remote centers. Forecasts are being made that the alarming and acute shortage of engineers to design these critically needed analog products, particularly high-frequency monolithic integrated circuits (IC) for use in numerous wireless, cable, and fiber-optic communications systems, will only worsen in the next few years.

A high proportion of these products support the day-to-day operation of the Internet, which is rapidly becoming the epicenter of commerce, as well as a global meeting place and the repository of vast amounts of information, and whose phenomenal success must be placed alongside the chance discovery of bipolar transistor action [1], the invention of the planar process [2], and the development of CMOS [3], [4] in having changed life on Earth in profound and far-reaching ways. It is apparent that semiconductor processes and the products they support are destined to become a permanent aspect of everyday life, touching even more deeply on the lives of those millions of people who have yet to break through the political and economic barriers currently blocking unfettered access to advanced technology. Not only in the West, but even in remote villages in India, the insatiable appetite for fast data has made the term *bandwidth* a household word, although few understand that the proliferation of this much-desired “digital” commodity will be attained through further advances in *analog* techniques. The insatiable demand for bandwidth, whether supported on wires, in optical fibers or through the ether, will challenge designers of communication channels for many decades to come. Fundamental analog functions—including amplification, the generation of oscil-

lations of high-frequency accuracy and signal purity, carrier power generation and control, sometimes involving sophisticated linearization techniques, the provision of accurate selectivity and linearity at precise and often very high frequencies, frequency translation, modulation and demodulation—will remain an indispensable part of these physical channels, which, whatever the label on the box, will be largely *Analog Inside*.

In view of the foregoing, it is timely to review the state of the analog art and attempt to identify at least some of the limits to progress. Many questions come to mind and each could easily be the topic of a full-length paper: Why and in what way are analog circuits and their design so different (some would say “so hard”) compared to digital design? How can we cope with the complex *multidimensional tradeoffs* and compromises that arise in any design endeavor, but which are particularly challenging in analog circuit optimization? What are the fundamental limitations to such basic performance parameters as bandwidth and linearity? (The limit to minimum attainable noise is much less uncertain.) What semiconductor processes are going to be used for these circuits? Will supply voltages drop below today’s levels, typically in the range 2.4–5 V? What must be forfeited if analog circuits are forced to migrate to the 1-V supply level, enforced by the limitations of advanced CMOS processes developed primarily for digital use? Can we expect to see a sustained divergence in silicon fabrication processes for digital and analog applications, offering well-optimized elements for these very different realms of endeavor? Or will the analog designer be forced to wax even craftier in employing cruder logic-optimized active elements to address prevailing *physical* performance objectives? Will other semiconductor materials become not only useful, but essential in certain areas of analog signal processing? Of course, only a few of these questions can be addressed here.

Section I examines the analog art of today and outlines the enduring differences between analog and digital design. Section II reviews the topic of mixed-signal integration and the system-on-a-chip initiative and suggests that pragmatic alternatives may make more sense. Section III attempts to peer through the cracks in the construction fences surrounding the future. The course followed in this paper in unashamedly skewed toward a consideration of the role of bipolar technologies, which is not quite as serious an anachronism as it may at first seem since it remains true that these remain of critical importance and new processes continue to be developed. The example used to show the curiously tantalizing correspondence between carrier statistics in a semiconductor and BJT circuit behavior are offered with a grain of salt only to underscore the more reliable basis of bipolar transistor theory, compared to the more empirical nature of surface-conduction devices. It is intended to be thought provoking rather than definitive, as are many of the strong assertions scattered along the way.

I. ANALOG TODAY

Analog circuits are closer to nature than are digital circuits. This sweeping assertion is neither a sentimental

whimsy nor a philosophical distinction. It is the essential starting-point of a clearer understanding of why these two domains of endeavor are fundamentally so different. There are actually *three* fields of electronics today: the two major groupings, analog and digital, and a third, smaller but well-defined and rapidly growing group of techniques which we can call *quasi-analog* or *binary-analog*, exemplified by “sigma-delta” techniques. The three basic disciplines overlap strongly and are codependent: they are at once symbiotic and synergistic. Many of the challenges in digital electronics today have a strongly analog aspect, mostly, of course, at the cell level. These stand apart from the more important development thrusts which relate to the transformation of binary data, treated in an almost abstract fashion, and in which the sequential discrete algorithm replaces the unfettered autonomy of the analog circuit.

A. Dimension and Reality

We can say that analog circuits are more deeply a part of the physical world because, first and foremost, they are concerned with the manipulation of signals having *dimensional* attributes, traceable to fundamental physical constants. The primary physical units are length $[L]$ in meters, mass $[M]$ in kilograms, and time $[T]$ in seconds, and we here use charge $[Q]$ in coulombs as the fourth basic unit.² The *physical algebra* of analog-circuit analysis differs from ordinary algebra in that it always contains embedded references to these constants and demands strict attention to *dimensional homogeneity*. This crucial requirement permeates the design and analysis of analog systems, while being irrelevant to digital design.

Thus, signals in the form of *voltages* carry the dimension of $[ML^2T^{-2}Q^{-1}]$. In other areas of a circuit, greater importance might be attached to the *currents*, which are of dimension $[QT^{-1}]$. Voltages are just another way of representing *energy* $[ML^2T^{-2}]$ normalized through division by the *electron charge*, while current may be envisaged as counting multiples of charge quanta over a specified *time* interval. These quantities are inextricably woven into the fabric of the universe, from subatomic forces up to the largest cosmic objects. RF signal levels in a transceiver can be equated to an electromagnetic *field strength* at the antenna and expressed as a *power* $[ML^2T^{-3}]$ at some *frequency* $[T^{-1}]$. Similarly, the electrical elements within which these signals flourish and propagate have their own unique set of physical dimensions: *resistance* $[ML^2T^{-1}Q^{-2}]$; *capacitance* $[M^{-1}L^{-2}T^2Q^2]$; and *inductance* $[ML^2Q^{-2}]$. The attribute of *spin* $[MLT^{-1}]$ is an essential aspect of semiconductor device behavior, as are the *mass* $[M]$ and *velocity* $[LT^{-1}]$ of holes and electrons, and of course the pure *length* $[L]$ of device structures. In view of this strongly physical nature of analog circuits, it is fitting to use the term *Newtonian* to describe them.

The quantity known as the *saturation current* of a junction device, I_S , is traceable to a more basic quantity, the intrinsic carrier concentration, n_i , a direct manifestation of transition

²The International System of Units (SI) uses the Ampère, rather than charge. Charge is used in the present context because it is an intimate aspect of semiconductor physics.

probabilities (from which stem the *exponential* properties of junctions)

$$n_i^2 = 32 (\pi kT/h^2)^3 (m_e + m_h)^{3/2} \exp(-E_g/kT). \quad (1)$$

Note again the rich connections to the physical world. In this one expression we encounter temperature T (Kelvin); the Boltzmann constant k (1.3807×10^{-23} joules/Kelvin); electronic charge q (1.6022×10^{-19} Coulombs); the Planck constant h (6.6261×10^{-34} Joule-seconds); the band-gap energy of silicon E_g (1.206 eV at 0 K as determined by optical absorption methods, but a somewhat lower value may be appropriate in certain equations, to account for doping, temperature and other effects); and the effective mass of the hole, m_h , and electron, m_e (these are actually *tensors*, whose magnitude depend on the direction of carrier motion in the lattice, amongst other things). There are cameo appearances of the real numbers 2, π , 3, and 32.

There is an almost mystical aspect to this wondrous quantity, and its progeny, I_S , which might be called the *soul* of a junction transistor, since so much of the transistor's personality stems from this deep foundation. Meanwhile, the *heart* of a p-n junction is the unique equation linking terminal current and voltage. A bipolar junction transistor (BJT) exhibits a strikingly simple relationship between its collector current I_C and the base-emitter voltage V_{BE} , which is captured pretty well by

$$I_C = I_S \exp(V_{BE}/V_T) \quad (2)$$

where $V_T = kT/q$ is called the *thermal voltage*, that is, the *thermal energy* of the lattice, kT , expressed in volts by normalizing to the electronic charge. As one might expect, this is not quite exact, and several excluded factors influence I_C in subtle ways. For example, V_T is multiplied by the *emission coefficient*, a factor which eventually becomes two at extremely small and large currents, but is close to unity over most of its operating range (generally being less than 1.005) and highly predictable from one wafer lot to the next. But its pragmatic value lies as much as anything else in its simple message; it is one of the *icons* of junction-device behavior.

From this equation, it immediately follows that the transconductance is

$$gm = \frac{\partial I_C}{\partial V_{BE}} = I_C/V_T \quad (3)$$

that is, the *transconductance is an exactly linear function of the collector current* and has nothing to do with the size of the device (its scaling), or even the semiconductor material (Si, Ge, GaAs, SiGe, etc.). These two equations, and a third, which simply recasts (2) to show the base-emitter voltage as a function of collector current

$$V_{BE} = V_T \log(I_C/I_S) \quad (4)$$

and which unlocks the door to *logarithmic signal processing* are reliable over nine orders of magnitude of collector current (a 180-dB dynamic range), for example, from 10 pA to 10 mA for a single, suitably scaled transistor fabricated on an IC process optimized for instrumentation applications.

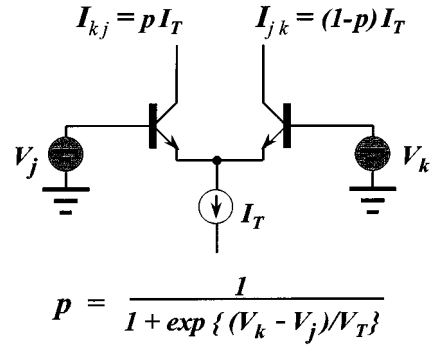


Fig. 1. Bipolar differential pair. A working model of Fermi–Dirac statistics?

This is nothing short of amazing and led the author in 1975 [5] to coin the term *translinear* to capture the essence of this marvelous aspect of the BJT (nowadays shared with the *heterojunction bipolar transistor*, the HBT, by direct application of the same basic theory). Since then, a distinct domain of translinear design has developed [6]–[8], including the subdomains of *dynamic translinear cells* [9] and *log-domain* signal-processing [10].

A remarkable illustration of the fundamental connection between BJT circuit behavior and the embedded physics is provided by the differential pair is suggested in Fig. 1. It is easily shown that the “tail” current I_T divides into two components in a particular, exact fashion, which depends only on the base voltages V_J and V_K (the “energy difference”) and in such a way that it is not too fanciful to speak in terms of a *probability* P of finding a carrier in the left-hand or right-hand branch, that is, the individual collector currents, which obeys to the Fermi–Dirac distribution function

$$P_{\text{LEFT}} = 1/\{1 + \exp(E_K - E_J)\} \quad (5a)$$

$$P_{\text{RIGHT}} = 1/\{1 + \exp(E_J - E_K)\} \quad (5b)$$

where at the semiconductor level E_K and E_J represent the corresponding energy states between which the probabilities of a transition apply. In other words, this circuit provides us with a sort of “*working model*” of the statistical equations that govern conduction in a semiconductor material! This is not to say that the equivalency is exact or meaningful: it is just an *analog* to ponder.

We generally state (5) in this more familiar form, in which $\Delta V = V_J - V_K$:

$$I_{C1}/I_T = 1/\{1 + \exp(\Delta V/V_T)\} \quad (6a)$$

$$I_{C2}/I_T = 1/\{1 + \exp(-\Delta V/V_T)\}. \quad (6b)$$

This reduces to

$$\Delta I = I_{C1} - I_{C2} = I_T \tanh(\Delta V/2V_T). \quad (7)$$

The analysis of BJT circuits gives rise to equations involving such important functions as exp, log, tanh, sinh, and cosh. Using reliable translinear techniques it is easy to synthesize all manner of linear and nonlinear analog functions with impressive accuracy. For example, one can:

realize wide-band variable-gain amplifiers [11]–[13]; implement real-time multiplication and division of two or more variables [14], [15]; compute squares and square-roots and extract the rms value of a voltage [16], [17]; measure signal amplitudes at microwave frequencies [18]; compute vector sums and differences [19], [20]; generate sine–cosine functions [21], or all the trigonometric functions, (sine, cosine, and tangent, the reciprocal functions cosecant, secant, and cotangent, their inverses and a few more functions, such as versine and haversine)—*all* within the confines of a single monolithic circuit [22]; generate an output which is very exactly equal to the logarithm of an input, thus represent signals in decibel form [23]; generate an N -wide output array $\mathbf{B}(k)$ whose elements are proportional to each value in the input array, $\mathbf{A}(k)$, virtually instantaneously, even for large N (e.g., 100 channels) [24]; and implement analog read-only-memories [25]. These are just a few examples from the author’s own experience. A more comprehensive survey of the literature (which this paper lays no claims to being) would include very many more.

This extraordinarily dependable behavior suggests that we may think of the BJT as the *mathematical* transistor: its behavior is defined by just a handful of fundamental yet simple equations, whose sockets lie deep and securely in the nature of atomic structure. Translinear circuits provide a good example of the essence of the analog art, namely, a total reliance on exquisite details of device behavior. This is both an asset and a liability of course: an implicit dependence on parameter values inevitably brings in its wake an undesirable sensitivity to the slings and arrows of outrageous wafer processing.

A further example of a quintessentially analog principle is that of continuous-time feedback, which is not only a powerful force for the reduction of such sensitivities, but is also at the heart of analog computation. Thus, a large set of simultaneous equations can be solved almost instantly using nonlinear analog feedback techniques, of course, *without appealing to an algorithm*. Taking a leaf out of Marshall McLuhan’s thesis, we could say “The circuit IS the program.” Numerous examples of little-known modern-day analog computational elements could be cited. Surprisingly, perhaps, analog computers are alive and flourishing; we just do not call them by that name any more, in much the same way as we have ceased to refer to microprocessors as “electronic brains.”

B. Intractable Solutions

As a direct consequence of possessing what might whimsically be called “free-will” to exhibit an infinite number of states, even rudimentary analog circuits can pose difficult and often intractable analytical challenges. Thus unaware of the constraints of an algorithm (a striking similarity to natural organisms), their behavior results from the continuous, autonomous and almost instantaneous solution of the virtual equations embedded in the physical reality. Forced to comply with the physical rules, these circuits will find a solution even when mathematics cannot. For example, consider the only slightly modified current mirror [Fig. 2(a)] attributed to Widlar. If asked: “What is the output current, I_2 , given the

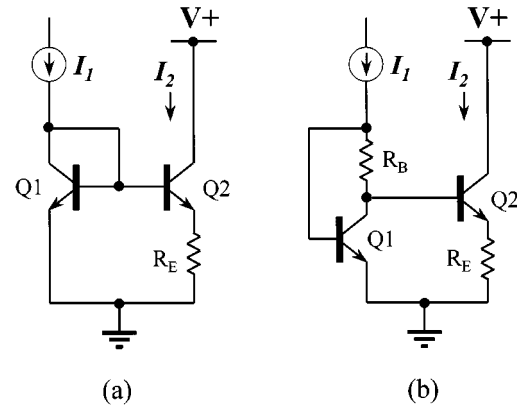


Fig. 2. Intractable circuits. (a) Widlar current mirror. (b) Variant.

input current, I_1 , the value of the resistor R_E and assuming equally sized transistors?” we could not offer a precise answer.

This may seem surprising, since cells like this are used every day, but it is nonetheless a common dilemma. It arises because the equation for I_2 is transcendental

$$I_1 = I_2 \exp(-I_2 R_E / V_T). \quad (8)$$

In this case, a design methodology is not hard to find, since I_1 is analytic: We could choose the desired output current, I_2 and emitter resistor, R_E , then calculate the needed value of I_1 . Or, we could solve for R_E , given I_1 and I_2

$$R_E = \frac{V_T}{I_2} \log \frac{I_1}{I_2}. \quad (9)$$

This illustrates a constant aspect of analog design: a topologically simple cell can be frustratingly awkward to analyze and optimize. The addition of only one more resistor [Fig. 2(b)] results in an equation that cannot be solved for either I_1 or I_2 , given the other

$$I_1 R_B + I_2 R_E = V_T \log \frac{I_1}{I_2}. \quad (10)$$

Further, in advising a student reader to “Choose I_2 and R_E ,” how on earth are such choices to be made? How should one decide which of a very large number of possible transistor geometries, output currents and resistor values ought to be used? Even a one-transistor circuit, such an RF low-noise amplifier (LNA), can tax the patience of an experienced designer and consume many hours of optimization time during simulation and practical evaluation, when noise- and power-matching considerations have to be balanced against the need to minimize intermodulation, while keeping the supply current to a reasonable value. Judgment (which may be defined as experience-guided guessing) remains an essential factor, and an appeal to heuristics—the *What If?* route—is often more productive than a formal, systematic approach to problem-solving.

Many new analog cells continue to be invented (or discovered) using the same few transistors rearranged in some slightly different way, and frequently this new insight did not require any advances in process technology. For example, a

recent type of Class AB RF mixer [26] could easily have been invented in the 1960s, but had to wait until 1994, until the idea just happened to occur (shortly following surgery with a general anesthetic!). The ephemeral and unpredictable nature of invention is well documented [27]–[29]. In this case, the circuit topology was not new; it had appeared nearly 20 years earlier in one of the author’s own papers [5, Fig. 2b], in the guise of a vector difference circuit! What had to be awaited, in this case, was the realization that this utilitarian cell could also solve a basic problem in radio design, having to do with the compression in the conversion gain of a mixer, an application in a totally different domain and providing a markedly different function. It is quite astonishing how many distinctly new cell topologies continue to present themselves to an experienced mind, and it is often a mystery why they never occurred to one before.

The endless variety of analog cells and functions stands in monumental contrast to the limited variety and simple function of logic gates. Teaching a course called “*Creative Circuit Design*,” at a time when it was imperative to get the most action out of the least number of expensive germanium transistors, I delineated 24 *distinctly different* circuit functions that can be realized by two transistors, supported by a few passive components in some cases, as well as endless variants on each theme, depending on component values and operating conditions. The number of possible three-transistor circuits runs into the hundreds, and a meaningful synthesis technique quickly becomes improbable as more devices are added. Concurrently, the analysis of even simple circuits is often intractable. In this connection, it is notable that a close scrutiny of Widlar’s famous paper [30] describing his three-transistor band-gap reference cell will reveal that nowhere did he provide a closed-form expression for the output voltage as a function of the circuit parameters, because, here again (though he failed to mention it) there is no analytical solution.³

By the time one employs as “many” as ten transistors, the number of possible circuit topologies, device geometries and parameter values becomes truly formidable. Design and analysis in such cases may rely on an *effect-needs-cause* approach, rather than an appeal to the *cause-begets-effect* (event-driven) route. The deliberate reversal of cause and effect is a common requirement in the analysis of analog circuits, most notably in control systems employing one or more feedback paths. These may be: linear and memoryless (as is a resistive attenuator, where the property of greatest interest is the *ratio* of the elements); linear and reactive (to shape frequency or transient response); or nonlinear, in which case, further dimensional aspects are introduced.

The endless applications described in a plethora of books about operational amplifiers testify to this idea: in many cases, the op amp is operating less like an amplifier and more like an adjudicator, balancing the demands of all the elements connected to its summing node, and nulling their aggregate contributions. Its output is then “whatever it has

³That is not an essential aspect of band-gap reference design, however. The more commonly used cell devised by Brokaw [31] is analytic, as are many new realizations of the “band-gap principle” in BJT and CMOS.

to be” to make this happen. This is not the conventional way one thinks of amplifiers!

All nonlinear circuits and elements have embedded dimensional parameters which can be expressed as internal voltages and/or currents. Thus, the BJT equation (2) embodies a *current reference* I_S traceable back to the more fundamental quantities given in (1), and it incorporates a *voltage reference* V_T . Since all practical analog circuits are nonlinear, the impact of these are an inescapable aspect of design. Given insufficient attention, the scaling attributes of your circuit will be determined for you, by the rules of physics. Such lapses are common, and are in part responsible for the unfavorable reputation of analog solutions. In many a poorly conceived product, various empirical “corrections” were tacked on at the eleventh hour. Lacking a solid fundamental basis, the resulting parametric sensitivities mar production yields, or stability over temperature and supply extremes. The experienced designer ensures that the circuit is allowed little latitude to exercise independence. In the most successful designs, the methods used to achieve this degree of control are so deeply subsumed into the fabric of the circuit that they often cannot be pointed to, as a *separate* part of the structure.⁴

C. The Importance of Ratios

Although the significance of *dimensional attributes* in analog circuits has been stressed, some analog performance attributes are in fact dimensionless. Common examples include attenuation and gain; gain matching; phase and phase-matching; filter Q (relative locations of poles and zeros in the s -plane); duty cycle; etc. These are all simple *ratios*, and can be defined to high accuracy. Monolithic analog design depends strongly on the matching of like against like, and on the use of *replicated unit devices* to realize ratios immune to global delineation errors, and generally less sensitive to short-range errors, using interdigitation of subunits. Closely related is the expectation of isothermal operation, making these ratios almost entirely independent of absolute temperature.

A deep reliance on matching and isothermal operation permeates analog design. For example, in a BJT, the saturation current density, I_S , to which the collector current is proportional (2), varies enormously with temperature, by a factor of well over a *billion to one* for a typical range of operating temperatures. If V_{BE} were held constant, a similar variation in I_C would occur (in principle). However, this is of no consequence in a BJT current mirror: although $I_S (= A_E J_S)$ of both transistors varies wildly over temperature, the mirror ratio A_2/A_1 is unaffected. I_S also varies considerably from

⁴An example of this sort can be found in a cell topology for generating a band-gap reference voltage that is *fundamentally* free of curvature, that is, *not* by an appeal to a correction method [32]. In another case, the (unknown and variable) ohmic resistances, R_Ω , in each emitter of a BJT differential pair, which would normally lead to a reduction in small-signal gain, can be *automatically* and *exactly* compensated by using transistors having the same pathology in the bias cell (also [32]). In both cases, the solution is based simply on making correct choices for device geometries and component values.

one wafer lot to the next, due to changes in doping concentrations, junction depths, and the delineation of emitter area, yet the mirror ratio remains stable.

Similar considerations arise in CMOS analog design [33], where the use of replicated devices, having equal channel width W and length L , not simply an equal L/W ratio, is often mandatory. The use of a channel lengths much longer than the permitted minimum is also common, again with matching in mind. Monolithic analog circuits universally demand meticulous attention to cell layout, using, for example, common centroid techniques to minimize the effects of all first-order gradients (in doping concentrations, emitter delineation, temperature and mechanical strain) and fastidious concern for the consequences of metallization paths (resistance mismatches, voltage drops, mismatches in parasitic capacitance, field effects, etc.). Early op amps suffered from a type of low-frequency harmonic distortion caused by thermal feedback from the power-dissipating output stage to the sensitive input cells. Many other layout precautions are needed; some are even proprietary. We are still discovering some subtle new sources of device mismatch.

The *reliance on ratios* permeates all monolithic analog design, and led to the invention of many new circuit forms during the late 1960s and 1970s, formerly impossible using discrete transistors. In retrospect, it is hard to see why we often felt that a monolithic circuit would be lucky to match the performance possible using the discrete assembly techniques of the time. We had not yet learned how to apply the new design paradigm, or how to work around such things as a severely limited range of resistor values, the large temperature coefficients of diffused resistors (0.1%–0.2% per degree), the absence of capacitors of more than a few picofarads, and the unavailability of many of the components commonly used in discrete design.

Analog CMOS practice depends strongly on capacitor ratios. Foundry processes provide few, if any, high-quality resistor layers; often, they are of a low sheet resistance and high TCR. Furthermore, signals in CMOS circuits are often best viewed in charge terms, since it is easy to transfer packets of charge with high accuracy, as in switched-capacitor circuits [34]. These may require the use of a modified CMOS process when the capacitors must exhibit good linearity. Capacitors can match to very close tolerances. Unlike diffused and polysilicon resistor layers, they are insensitive to chip strain and have a low-temperature coefficient, which eases some layout constraints.

Switched-capacitor (SC) continuous-amplitude circuits represent analog variables as voltages. Thus, preserving a wide dynamic range requires the use of large signal voltages, not permissible in the most advanced CMOS processes. Such considerations may affect the mix of processes that can be used in future mixed-signal applications. The pressure to reduce the cost of analog functions has led IC designers to find ingenious ways to cope with the limitations of CMOS transistors optimized almost entirely for use in binary gates, by taking the reliance on ratios one step further and representing the signals in *time-ratio* form. This is the key insight in sigma–delta techniques [35], a concept that has

reached a remarkable level of sophistication in modern ICs. Using duty cycle to represent a continuum of analog values, and simple binary circuits to process the signal stream, the time quantization inherent to the technique can actually be put to good use in shaping the equivalent frequency-domain response to advantage.

Such techniques, used both for analog-to-digital and digital-to-analog conversion, have rapidly become standard in digital audio equipment. Classical analog considerations related to dynamic range are transformed into the uncertainty in duty cycle. That is, the noise floor is determined by time-smearing or jitter. Analog noise mechanisms are still the root cause of this, of course, and limit the dynamic range of a first-order sigma–delta system. Many of the advances in this domain are found in the *noise-shaping* methods [36] which address this problem in innovative ways. Frequency selectivity (filtering and tuning) and nonlinear functions can also be implemented in the duty-cycle domain. Since the information content in such processors is contained largely in the states of its constituent gates, the reliance on capacitors matching, as would be found in SC filters, is eliminated.

The use of ratio-based signals and binary processing elements defies unequivocal classification into either analog or digital. However, these techniques are likely to gain increasing use, as IC processes optimized almost entirely for logical signals provide diminished flexibility for analog design, and dynamic range is more severely limited by the reduced operating voltages. For example, we can expect to see an increasing use of sigma–delta DACs tightly integrated with Class-D power amplifiers in future home-entertainment audio systems. The design and optimization of sigma–delta systems is difficult using standard analog simulation tools such as SPICE, but new tools for the development of sigma–delta systems of all kinds are now available.

D. Limitations of Direct Data Conversion

The use of microprocessors and DSP to implement certain analog functions (such as filtering, modulation, and demodulation) relies on “data converters,” ADCs, and DACs. In recent years, these have enjoyed a remarkable rate of innovation, providing advances in basic performance (speed and resolution) with a dramatic reduction in cost and power consumption. Converters for low-speed applications are now a very mature art. Sigma–delta circuits have enormous potential for accuracy unhindered by the limitations of binary-weighted resistor and capacitor ratios. In audio and instrumentation applications, 24-b resolution is no longer a pipe dream.

The situation in high-bandwidth converters is not so fully resolved, and many challenges remain. The ultimate radio receiver has for many years been envisaged as one in which the full spectrum of signals at the antenna would immediately be digitized, with all the needed selectivity for channel selection subsequently implemented in DSP. Likewise, the transmitter would use direct digital synthesis of the carrier, in which the analog signal is generated using a DAC at the antenna interface. The appeal of these ambitious notions is obvious: once

this can be achieved, a single transceiver can be instantly re-configured for any type of service or set of communications standards, “merely” by changing some software. Initiatives of this sort have spurred the development of a new breed of data converters, often specified using such metrics as noise and intermodulation, formerly found only in the context of purely analog signal processing.

Progress toward this goal has been excellent. It is now common for digitization to occur in the intermediate frequency (IF) sections of a receiver, operating in the general range 10–300 MHz, and perform channel selection, demodulation, and the extraction of the data payload entirely in the software domain. The need for a high-speed converter can be avoided using a very low IF or by translating the RF spectrum directly to baseband, using *zero-IF* techniques. However, the front-end (the LNA and down-converting mixer in a receiver, and the up-converter, power amplifier, and power-management in a transmitter) will remain analog for the indefinite future, except where the received signal strengths are high and carrier frequencies and transmit powers are low, when direct conversion to and from digital data is feasible.

The development of the truly universal *software radio* is still a daunting prospect. Even for a single communications standard, such as GSM, the firmware needed to support all layers of activity in a cellular phone handset runs to many thousands of lines of specialized code, representing an expensive part of the development of a GSM chip set. A similar state of affairs is found in many contemporary radio systems. Optimism about the imminent reduction of such transceivers to a “single-chip solution” is, I believe, premature. There are reasons for suggesting that this will be neither practicable nor cost effective for many years to come, and perhaps never, if advances in low-cost assembly techniques overtake progress in the mixed-signal arena. Quick, effective reuse of less sophisticated, off-the-shelf solutions is more likely to be employed than the development of very complex ICs that attempt to cram numerous often disparate functions and disciplines into one ultimate solution. Only when the volume of usage runs into the tens of millions of pieces can such ambitious undertakings be justified, and not always then.

E. Other Limitations

In the analog domain, almost every parameter of a transistor has a direct bearing on some aspect of performance, and agonizing compromises and tradeoffs are necessary. In digital design, the emphasis is entirely on the use of transistors as rudimentary switches, needing nothing more than a decisive nonlinearity, with sufficient gain in the transition region to ensure bit regeneration, and the lowest possible inertia. There is generally little need for concern about thermal noise generation in the preservation of digital accuracy. Rather, the total number of atoms in a digital gate or memory cell is desirably minimized as far as possible, until the incidence of soft errors induced by particle hits, and eventually by quantum fluctuations, become excessive. Ironically, it is the very use of quantum effects that may open the door to a new era of computation, but effects of

a totally different kind to the random thermal motion of carriers in a crystal lattice.

By contrast, one invariably needs to ensure that a *large enough* number of atoms are used in an analog device to ensure adequate matching accuracy, low ohmic resistances (to reduce Johnson noise), and the capacity to sustain high current levels. However, just as in a digital cell, inertia (caused by charge storage) is a major concern, again demanding the use of small device geometry. Such issues as harmonic distortion and intermodulation mechanisms also lead to conflicts in device sizing. The nonlinearity of junction capacitances, for example, contributes to HF distortion, suggesting the use of small devices, while ohmic resistances can generate distortion in many common translinear circuits, and noise in all types of circuit.

Dynamic range is a well-known fundamental limitation in analog design. Numerous factors conspire to degrade this crucial performance metric. The most important of these are noise, in the modulation bandwidth, determining the lower extremities of dynamic range; intermodulation, the process by which multiple signals simultaneously present in a channel interact so as to generate phantom signals which appear to be genuine by the time they reach those stages in which the modulation payload is extracted; and occasionally, device mismatches, which may exacerbate certain kinds of distortion, cause undesirable imbalances in signal levels and bias points, lead to gain errors, and so on.

Here again, in sharp contrast, dynamic range is a simple concept in DSP, embodied in word length, *not circuit performance*. It can, in principle, be as large as one wishes, and floating-point processors can readily cover magnitude ratios far greater than found anywhere in the physical universe. The notion of “digital noise” is also significantly different, referring either to accumulative truncation errors in an algorithm, or to deterministic (and sometimes periodic) hash at the gate level, rather than stochastic events of thermal origin, although the latter are not entirely negligible, and will doubtless become even more troublesome as scaling continues downward. Intermodulation has no corresponding equivalence, and device mismatches are usually far less troublesome, although they may have an adverse effect on timing delays and race conditions.

II. THE MIXED-SIGNAL CHALLENGE

The invention of the telegraph, the telephone, and wireless were but the opening fanfare heralding an new era in which the world was about to change beyond recognition, by linking together not just geographical territories, but eventually ideological ones, too. Profound changes in the very nature of human life will continue to be wrought by electronics.

The most striking aspect of this drama today is the *confluence of radios and microcomputers*. Only recently, these were separate areas of endeavor, the old analog and the new digital, but they are converging because economic forces dictate it, and because the stunning advances in semiconductor

technologies have opened up the possibility of their synergistic cointegration, in monolithic ICs of intimidating complexity yet low cost. *This is the mixed-signal promise.*

This radio-computer fusion has already attained limited success, in cellular phones that handle not just voice traffic, but numerical data and graphics, with video capabilities soon to follow. The potential of digital data to convey any sort of information has blurred the distinction; they are all merely *applications*. Such ubiquity is understandably at the root of the claim that “everything is going to be digital in the future.” And this, so goes the popular belief, includes radios.

A. The System on a Chip

While digital techniques now penetrate more deeply into the fabric of transceivers, one only has open to up a cellular phone to realize that there is an enormous amount of board space consumed by the radio system, and that many discrete components, including even a few transistors, are still used. This is not a cause for celebration—vindicating evidence that analog is not ready to be retired—but simply a striking reminder of how very difficult it is to reduce these sections to the much-heralded *system on a chip*, or SoC.

This is a term that begs precise definition, since any collection of elements is a system. In some contexts it can mean a large, purely digital system, but it is also used to refer to an IC containing all the parts needed to realize a complex function entailing both analog and DSP. Aggressive claims as to the imminent advent of the single-chip phone, being made during the mid-1990s, were premature. There remain many difficult hurdles ahead, and these are readily appreciated by the designer of small analog circuits, such as the ultralow-noise amplifiers and VCOs that are essential elements of a sensitive receiver working at frequencies of 2 GHz and above. RFIC designers know that even if one slightly alters the pin sequence around the package, or the way the die is positioned on the header, performance may be impaired. Consider that the smallest signal that must be detected while still providing an acceptable bit error rate (BER) is typically only some 40×10^{-15} W (−104 dBm), amounting to 1.4 μ V at a 50- Ω antenna impedance, about a millionth of the voltage swing on the hundreds of thousands of digital gates that will be buzzing away a few millimeters distant on the same substrate. This is the *mixed-signal challenge*.

As well as the sheer physical challenges of SoC design, there is the issue of bringing together all the needed skills in a common environment. The strongly disparate tools that are favored by the analog and digital partners—usually SPICE derivatives and specialized RF design tools for the former, and VHDL for the latter—stand in the way of this sort enterprise. These obstacles have received a great deal of attention, during many years of meetings of the IEEE-1076 working groups, who have been struggling to define an extended language called VHDL-AMS [37], but much remains to be done, and a full solution will require the wisdom of Solomon. The use of “top-down” design within the framework of what remains a purely mathematical representation—burdened by the need to fit the structure to a single semiconductor process and reliably anticipate all the

effects of device scaling over a broad range, including the use of foundry processes that may have been only recently developed—is a very tall order and quite different from the way in which analog systems have traditionally been developed over a period of some eight decades.

Further difficult challenges arise in the *testing* of mixed-signal products, partly from physical considerations (measuring the fine-scale performance of the radio system in a production handler alongside the rattling cages of the same IC’s digital partition) and partly from the need for verification of a system that can exhibit a large number of potentially unacceptable design faults (in the circuits and the firmware) and production flaws.

It is noteworthy that high-frequency analog ICs are often poorly characterized. Data sheets assign many of the key specifications only a *typical* value, with no guarantees of their minimum and maximum limits. One may occasionally be given the six-sigma distribution on some of the easily tested parameters, such as supply current. The board-level engineer is expected to make do with “*Performance Curves*.” RF designers are used to this imprecision. Inevitably, pragmatism and desperation set in, and the problem is thrown into the arms of fate: the construction of a prototype. For those with an appetite for the very difficult, a career in mixed-signal development—whether of the design tools, the products themselves, or the testing methodologies—is bound to prove exciting.

The basic question of whether one technology can “do it all” deserves careful consideration. The quest for monolithic implementations of every electronic function, no matter how complex or arcane, has become a kind of test of strength, the rites of passage. Cost is usually cited as the reason, though the intrinsic excitement of the hunt is often as important. Being the first to announce “*A Fully Monolithic Solution to a Very Hard Problem*” generally places the author(s) in a short list for a best paper award at the ISSCC. But, when all the numerous factors that go into the launching of a successful product, including meeting all the performance goals, time-to-market, testability, suitability to the application, freedom from bugs, and a few concessions to yield are all taken into account, is it the most *sensible* solution? Is it even the *cheapest* solution? That used to be true of all monolithic circuits, *but the rules are changing*.

There is a great deal to be said for bringing together whatever specialized technologies are optimal for each subsection, using advanced assembly techniques that infuse a new vitality into the old hybrid methods. This may seem retrogressive, at a time when we are doing so well with ever larger VLSI. However, that is misleading: the dazzling advances in this field are limited almost entirely to *purely digital* systems, occasionally augmented by some low-speed data converters and a few simple amplifiers. We have yet to see the definitive breakthrough in a transceiver SoC, including full integration of the RF front-end, PLL-controlled VCO, power amplifier and its power control, along with all the required filtering DSP, codec, physical-layer controller, and the microprocessor and memory needed to run the show and send the bill.

These are some of the problematical elements of the contemporary SoC scene.

- 1) Major challenges stand in the way of integrating sensitive analog sections with digital sections, including: the isolation of sections having high-gain bandwidth; spurious signal injection; VCO phase-noise disturbances; PLL locking errors; elevated noise figure due to the operating temperature of CPU sections, etc. CMOS inverter-style logic will be especially troublesome because of large, fast current spikes, generating magnetic EMI pulses, as well as voltage drops in the interconnect and throughout the substrate, which appear in analog sections.
- 2) Highly disparate demands are placed on a common technology, which may be supplied by a foundry with a limited appreciation of (or interest in) the special issue of analog modeling, or the negative consequences of small changes in the production flow aimed at improving mainstream digital operation. Much has been achieved in applying submicrometer CMOS to RF circuits, but performance requirements often lie beyond what can be delivered by a "one-size-fits-all" technology, particularly one that lacks many of the traditional strengths of analog IC processes.
- 3) High integration levels inevitably result in some reduction in yield. In a complex SoC, yield will be dragged down dramatically by the parameter-sensitive analog sections, which may account for only a few devices but a disproportionate chip area.
- 4) Complex multifunctional chips complicate testing both in terms of methodologies and the needed entourage of instrumentation dedicated to a given production line.
- 5) The combination of many novel kinds of pure-analog circuitry, plus switched-capacitor and sigma-delta analog cells, alongside established digital libraries, poses huge challenges to the EDA industry. The design tools for mixed-signal design are still very much in a state of flux and considerable uncertainty remains as to how these will evolve. Even the best simulation software for pure-analog design is unable to fully cope with many contemporary situations in an adequately realistic fashion. The simulated operation of all parts of a complete mixed-signal system of even moderate complexity taxes the fastest available computers, and any hope of using full Monte Carlo studies has to be set aside.
- 6) The issue of simulation tools of adequate power is closely allied to that of providing device models of adequate accuracy. In RF design it is common to use super models for all elements, including passive components. These add many extra nodes to the circuit and also require careful attention to local substrate potentials, the impedance of interconnects, and other coupling mechanisms (e.g., mutual inductance). Thermal modeling and meticulous layout frequently needed in crafting pure-analog circuits might be

neglected or completely overlooked in a mixed-signal production.

- 7) Complexity places immense demands on mixed-signal teams. Developments become transformed from formerly technical challenges to management problems, adversely impacting time to market unless scheduled with military precision.
- 8) For very large production runs, the high development cost and risk may be offset by low unit cost; but cost reductions might also be possible if some of the effort now being lavished on the monolithic SoC were spent on alternatives.

B. System in a Package

Consider, by contrast the benefits of what we might call the *system-on-a-header* (SoH), or the *system-in-a-package* (SiP), that is, the combining of disparate technologies in the form of pretested chips, sometimes along with specialized passive components, using highly automated assembly techniques.

SYNERGY: Optimal IC technologies can be employed: being built up from individual IC units, any contemporary technologies may be included in the SiP. The need for design compromises is eliminated.

FLEXIBILITY: New systems may be quickly configured on demand, with short turn times; both major and minor design changes can be made with a high probability of success. SiPs are inherently evolutionary, rather than calling for a major rethinking of architecture and layout in the development of each new system; they can benefit from constant improvement and refinement.

VARIETY: Difficult RF elements, such as directional couplers and combiners, specialized filters, high- Q tanks for low-phase-noise VCOs, and passive components such as high-value decoupling capacitors, inductors and varactors, now become viable candidates for integration. MMICs using technologies such as GaAs, which are totally alien to the digital world, and which defy assimilation into a foundry process for very physical reasons, can be included as readily as a power amplifier die, using a P-HEMT process, or a low drop-out regulator on a pedestrian bipolar process.

ISOLATION: Critical sections are readily isolated using a relatively thick metal substrate of high conductivity, providing improvements in both electrical and

thermal isolation. The component chips may be physically arranged with less concern for the matter of interconnection on a single complex die.

TOOLS: Simple, proven, and effective design tools for analog design and high-level VLSI tools can each be used where needed, with full continuity.

TEST: The component dice are inherently much simpler and may be thoroughly tested in available handlers and using well-developed, debugged software and only moderate amounts of general-purpose instrumentation; unlike the specialized test bays for SoC, these may be shared with other products in the line. Final testing of the packaged system will always be required, but this can be relaxed to little more than the verification of successful interconnection and basic operation.

YIELD: Using standard statistical methods, we should expect to achieve a higher net yield when each component chip is only moderate in scale.

TTM: For obvious reasons, the time-to-market can be much quicker than a full SoC development. The stresses imposed on a large team can be largely eliminated.

REUSE: Numerous existing, *fully proven* dice, in the form of reliable products, from which design flaws and pathologies have been purged, may be utilized. The risky translation of cells concepts into totally new contexts is eliminated.

RISK: The SiP is no longer one very large and very complex die, but a fully accessible assembly of small units. Therefore, mistakes in the SiP substrate layout or other design indiscretions can quickly be located and corrected at low cost.

UNIT COST: If such automated assembly processes could be developed, and the handling of pretested bare dice perfected, it is likely that the *overall* fully amortized unit cost will be at least comparable to that of a monolithic SoC and possibly lower.

Until such assembly methods come along, advocates of the mixed-signal SoC will maintain that such methods are quite unnecessary, that the cost will always be prohibitive, and that the whole notion is retrogressive. It will be apparent that investment in this equipment and the SiP philosophy *will* demand a considerable stretch of the imagination and a good deal of faith in a favorable outcome. Meanwhile, huge sums of money will doubtless be poured into the development of many more attempts at monolithic mixed-signal systems, and

it would be less than charitable to wish these ambitious efforts anything less than fully deserved success.

C. Analog Design Reuse

In mixed-signal design, the desire to use proven and robust cells with little modification is understandable, since it promises to save time and lower risk. Design reuse is essential, safe and commonplace in the digital domain, where a processing element is to a considerable extent an event-driven state machine, and the loading rules are simple. The situation in analog design is radically different. Often, designers open themselves up to the criticism of being incurable tinkerers, never willing to leave a previously used cell design alone. They would respond by pointing out that, say, a band-gap voltage reference designed for Project A was perfectly well suited to that situation, but for Project B, it is necessary to provide much lower noise, or tighter accuracy, or drive a higher load capacitance, or any one of several other slight, but nonetheless significant, changes to achieve an optimal fit to the new situation. Fine-tuning of this kind seems inescapable, unless major concessions to performance, along a particular axis, can be tolerated.

Analog design reuse can fall prey to another fate. This happens when a less experienced designer accepts a cell verbatim, and applies it to a new set of circumstances with complete confidence as to its suitability, and in the person who concocted it in the first place. Even worse, in an attempt to add a little originality to the work, the neophyte may make a “few changes” without a deep understanding of the basic mechanisms, or a clear appreciation of the reasons why certain details of the design were included by the originator.

It is widely believed that common cells should be codified and captured in an expert system. Occasionally they can, and in the process provide some useful optimization tools for the expert user. However, problems arise when this kind of automation is used with little appreciation of how the results are generated. There is no satisfactory alternative to *mastery of one's medium*, and it should be the goal of mentors and supervisors to encourage the attainment of such mastery, rather than promote the use of surrogates for thinking. Why not propose that the young designer should write such a software tool, to gain experience with the issues, and then throw away the code?

The sort of recycling that is of greatest value in analog design is the reuse of *ideas*, the appeal to certain recurrent and pervasive *themes* and proven principles. Even though it may take longer, it is often far better to start with a completely clean sheet of paper (or, more likely, a blank computer screen) and build the cell literally from the ground up, and from the boundaries inward, based only on the *performance desiderata* and the *known properties of devices*. Frequently, this will lead to a completely new solution, and occasionally, a whole new class of circuits. Clearly, the freedom to create in this fashion, *ex nihilo*, is not always permissible, nor appropriate. The TTM pressures, and the need to minimize risk, may require one to take a circuit off the shelf and dress it up

for some new occasion. As always, a little common sense is needed. *There are no algorithms for success.*

D. Process Limitations in Mixed Signal

Electronics at Milestone 2000 is undergoing an explosive paradigm shift. New deep-submicrometer CMOS processes are relentlessly being developed to meet the demand for ever smaller switching transistors, which can operate at yet lower voltages and thus reduce the switching energy CV^2 . These advances are outlined in the latest SIA Road Map, which attempts to look 15 years into the future. It articulates a strong expectation that supply voltages for digital circuits will fall below 1 V and that microprocessors will employ 200 million transistors by 2005, using 0.1- μm CMOS technologies. Already, dynamic RAMs have passed the billion transistor mark. Placed alongside the one-transistor LNA or VCO, the differences in process demands and design methodologies are stark.

A gate is required solely to perform a *logical function*. Variables have only two possible states and the range of allowable voltages to represent them is large. A “LO” may be anything from zero volts to 25% of the supply, while an “HI” might span the range 75%–100%. The values are not critical, and of little consequence even if they occasionally wander into strange territories. While obvious, the *dimensional nature of the voltages is totally irrelevant* to a logic gate. Likewise, the displacement currents which flow in the gate terminals have no inherent significance; they are merely the inescapable consequences of real devices. Of course, these transient currents, including their effect on the time delay through the gate and the average supply current, and on timing in a digital processor, and race conditions and much else will invariably be of great practical importance. However, there is no *message* conveyed by these aspects of digital signals. Likewise, the use of *ratios* in device scaling has no relevance to the signal; its use is limited to satisfying certain design objectives, such as centering the voltage threshold of inverter-style logic gates, or to address the need to drive the parasitic capacitances of clock lines and interconnections.

Digital systems can be designed (and often are) by engineers skilled in disciplines that are quite distant from electronics. This is particularly true of VLSI, where systems of great complexity are manipulated using languages and tools having scarcely any connection with electronics. In an important sense, a digital processor is only *incidentally* electronic. If it were not for the fact that silicon processes are cheap and the circuits very fast and tiny, other means might have evolved. Of course, digital circuits are easy to interface with numerous peripheral functions having a significant amount of analog content, as in the mixed-signal arena. Other technologies, should they ever become commercially viable, might need to forgo that advantage, and call for the invention of alternative bridges.

It is unlikely that new technologies will replace silicon-based electronics in digital applications for at least twenty years, although this prospect is the subject of many ongoing research projects, such as MIT’s printable circuits [38]. New

paradigms for computing, such as the use of quantum superposition, are decades from being commercially relevant, and still lean on electronic interfaces. We can say with confidence that silicon processes will continue to support analog, digital, and mixed-signal product alike. But what processes?

III. THE OUTLOOK FOR ANALOG

The youthful discipline of electronics has only just begun to explore the numerous opportunities for analog techniques. Rather than rendering these obsolete, the recent explosion in digital communications systems has only increased the demand for fully analog and mixed-signal products and solutions. Bipolar processes and design techniques are likely to remain of central value in analog products for years to come, basically because of their unique translinear properties, from which stem many possibilities that have become taken for granted over decades of use, and are which are embedded in numerous well-understood and proven cells.

However, contemporary production CMOS processes are beginning to catch up in certain respects, such as the provision of transconductance (gm) values, in large devices, not much lower than the channel current I_{DS} divided by kT/q , comparable to the limit value ($I_C q/kT$) provided by the BJT. This is not to suggest, of course, that this particular aspect of device behavior is the only one of importance; nevertheless, it has been one of the chief differentiators in the past. Traditional analog topologies continue to be of indispensable value in an increasingly large number of applications, particularly in the burgeoning wireless, cable, and fiber-optic domains, where the provision of high gm along with low inertia is often crucial.

A. Processes for Mixed-Signal Analog

The advent of silicon germanium heterojunction (SiGe HBT) technologies has spurred a renewed awareness of the enduring value of bipolar processes. The SiGe benefit springs partly from band-gap engineering techniques [39], which allow higher base doping concentrations, and thus lower base resistance, while maintaining a high-emitter efficiency, and simultaneously introducing a small accelerating field in the base to reduce transit time. Incidental benefits include a higher dc beta and early voltage. Claims for improved HF linearity have also been made, although there is a need for further impartial studies to confirm such benefits. SiGe fabrication may use ultrahigh vacuum chemical vapor deposition (UHV-CVD) to grow a base film layer [40] of accurately controlled thickness, and with the added benefit of tighter control of profile in the crucial base region of a BJT. Recent advances in SiGe heterojunction technology have led to f_{MAX} values in excess of 100 GHz [41]. The general outlook is that the SiGe transistor will ease some of the basic device design conflicts that have gradually limited bipolar performance in other directions, while in the pursuit of sheer speed, but it should be regarded as essentially evolutionary in nature.

On the other hand, many engineers today feel that they have no need for bipolar devices, even in demanding analog

applications, and it is certainly true that innovative ways of overcoming the limitations of digital CMOS processes in analog applications are being found on a regular basis. Nowadays there is a better appreciation of the need to approach CMOS analog design on its own terms, rather than forcing-fitting the design to conform with earlier bipolar techniques. For example, rather than making a band-gap reference using the junctions of two or more parasitic PNP transistors, ill-suited to such applications, there are now dynamic techniques, using a single junction and a sequence of two or more applied currents, of different values, and switched-capacitor amplification and demodulation to derive the reference voltage. The use of switched-capacitor and charge-shuffling techniques, in which CMOS transistors operate in their “native” mode, as switches, is very common. Many of the quasi-analog design techniques now in use, such as band-pass sigma-delta converters, did not exist only a few years ago, or were underdeveloped and awaiting suitable technologies for their economic utilization.

The justifications offered for using CMOS are invariably: 1) the low cost of the process; and 2) the ease of cointegration with digital logic. However, a complex process, supporting the passive elements often needed for analog applications, and in some cases, transistors having differing threshold voltages, is comparable in cost with a bipolar process, and, as noted earlier, mixed-signal circuits often demand a greater variety in device types than afforded by all-CMOS processes. For many functions of modest complexity, the die cost may represent a relatively small part of the total cost of delivery (engineering development, packaging and testing, customer support) and in such cases the rationale for using CMOS is less apparent, for a manufacturer having a wide variety of technologies available. Obviously, this would not be true for a “fabless” design company. The more important reason for the increasing usage of CMOS in analog design is that these technologies are widely available from many sources. This is especially valuable in universities, some of which no longer include bipolar transistor theory in their curriculum. Universities also thrive on research challenges, such as the possibility of building radios and other classical analog systems using ill-suited and unproven technologies.

However, apart from the excitement of finding ways around their inherent limitations, there are also substantial performance benefits to be enjoyed from CMOS transistors in numerous analog applications. While the logarithmic-exponential (translinear) properties of the BJT are invaluable in numerous situations, they are just as often problematical, particularly where distortion and intermodulation are a major concern. The relationship between channel current I_{DS} and the gate voltage over threshold, $V_{GS}-V_{TH}$, is often stated as being quadratic, and this is approximately true for long channels. Such a transconductance form is less prone to generating all kinds of distortion products than an exponential transconductance. For short-channel devices, the power law is even weaker than quadratic, which further improves the linearity of the transconductance taken as a separate property. This benefit is not always realizable, however, when the less linear output characteristics

(I_{DS} -vs- V_{DS}) are taken into account. The absence of shot noise in majority-carrier transistors is also a key advantage, though other noise sources remain problematical.

For mixed-signal applications, BiCMOS processes allow the use of a large portfolio of proven bipolar cells combined with the unique value of CMOS devices in areas where linearity is of critical importance. This represents an asset, at a moderate increase in wafer cost. Furthermore, the (almost) unique properties of CMOS devices as voltage-mode signal switches complement the BJT as a current-mode switch and adds a powerful new dimension to signal management. This is also true of the essentially zero-current gate electrode in analog signal-storage applications. BiCMOS processes can open the door to synergism arising from cell topologies which combine the two device types cooperatively. The preservation of the bipolar content offers a bridging function for the many skilled IC designers who are not yet fully comfortable with CMOS techniques. Finally, of course, the CMOS is available for all manner of logic applications, which are gradually becoming an indispensable part of modern ICs. Unlike a CPU, where the device scaling must unquestionably be state-of-the-art, the requirements in a mixed-mode IC are usually less demanding and can be addressed by less aggressively scaled transistors.

The question therefore arises: If BiCMOS is to be the platform of choice for future all-analog and mixed-signal applications, what is the appropriate CMOS node to which the bipolar component of the process should be added? Several considerations suggest that the 0.35- μm or perhaps 0.25- μm node will be adequate. First, there is of course the issue of cost; no advanced CMOS process is inexpensive, so this is a relative matter. Now, manufacturing equipment for CMOS tends to be closely allied to a specific process, and optimized for a specific major customer. In an important sense, the “equipment is the process.” Below 0.35 μm , the manufacturing equipment and wafer costs increase sharply. Second, the need for extreme scaling in the development of mixed-signal ICs having a dominant analog content (signal conditioning involving amplification, continuous time filtering, frequency translation, signal generation, analog nonlinear functions, etc.) is absent. There remains a very considerable opportunity for analog ASICs of this sort, having important binary sections, but where the tradeoffs favor the provision of devices of higher quality, including excellent passive components and such assets as low-barrier Schottky diodes.

Third, the supply voltage limitations of deep-submicrometer CMOS stand in the way of using an extensive portfolio of design techniques in which, for example, several junction voltages are stacked. Thus, in a 2.7-V context, one may comfortably stack two V_{BE} s and one V_{CE} , and in some cases (3.0–3.3-V operation, low current, moderate temperature range) even add an additional V_{BE} . This provides a tremendous amount of topological freedom. However, a 3-V supply generally cannot be supported in a contemporary 0.18- μm process, immediately eliminating from the cell portfolio a large number of preexisting and road-tested BJT cells and yet-to-be devised BiCMOS hybrids. Fourth,

a reduction in supply voltage places restrictions on signal amplitudes, which are not quite proportional to this voltage, thus lowering the available dynamic range. With these considerations in mind, it seems likely that BiCMOS processes intended for use in a wide range of mixed-signal applications might well combine a 0.25- μm CMOS process with a 75-GHz SiGe n-p-n, complemented by a moderately fast, high-gain p-n-p and the full arsenal of supporting passives, with up to five levels of metallization, and trench isolation.

B. Opportunities for Analog ICs

We are barely the start of the history of electronics. We can be confident that radios are forever, and that there yet remains much to be achieved in the wireless arena alone. Other types of communications technologies will continue to emerge in the next few decades. Some of these uses can only be dimly perceived at this time. Perhaps a new paradigm for short-range radios will emerge from the use of impulse transmissions coded entirely in the time domain, discarding conventional carrier-based methods. Fiber-optic transmission, including dense wavelength division multiplexing (DWDM), are clearly high on this list of new directions. We should expect to see continuing expansion of the use of electronics (and what is loosely called nanotechnology) in the “infotainment” domain and in toys. (Micromachined accelerometers are already used in game controllers.) There is no question that automobiles and appliances will make increasing use of these advances in microelectronics and micromechanics, with a large dependence on sensors and analog-signal interfaces [42].

It is essential, in the formulation of a durable vision for analog techniques to grapple with such over-the-horizon trends, as well as the more tractable immediate opportunities. In this area of growth and opportunity, we need to be aware that there may be many gaps in our knowledge, and we need to be concerned about the deeper forces that are shaping the microelectronics industry. One will not find answers to questions about the future by focusing on the immediate and readily quantified short-term needs of the marketplace, or on the forecasts provided by the analysts, or by considering near-term technological limitations.

The rules are changing. It may no longer matter that you live elsewhere than in the land areas that lie within less than 100 km from a coastline, the area in which over 50% of the world’s production is concentrated. Mere distance is no longer a significant factor in communicating, and electronic technology for this purpose is no longer expensive or available only to an elite. For the first time in history, one’s location on the planet no longer limits one’s ability to communicate. Using low-cost, pocket-sized, battery-powered devices, we can talk, send e-mail, access vast amounts of information, and perform many kinds of work, anywhere in the world, whether this means among urban concentrations or on a mountain, in a jungle, in mid-Atlantic, or in polar regions. This modern-day miracle—it is hardly less—can be directly attributed to the ubiquity of radio systems based on integrated devices of increasingly perplexing analog and digital sophistication.

It is noteworthy that there is a new generation of communities now emerging that are going to pass directly from medieval living conditions to the rich connectivity of the 21st century. This change will bring with it a strong demand for electronics products of all kinds, and marks the arrival of a new trend: the enfranchisement of a vast number of people for whom such technology has never before been available. This will lead to a massive expansion in the demand for ICs. The leaders in this business will be the companies who are prepared to invest in the special competencies related to the high-complexity, high-volume products and who are willing to bet on the likelihood of a fuller participation in global economies among that 80% of the world population which has hitherto never enjoyed such a prospect.

In the domain of advanced medicine there is also clear evidence of the confluence of analog circuits and micromechanical devices, as sensors, actuators, drug delivery elements, and integrated chemical analysis systems, in monitoring and controlling biofunctions through RF devices [43]. We can, for example, envisage small pills which may be readily swallowed, and containing transmitters equipped with sensors for temperature, pH value and specific chemical molecules, which could become commonplace prescription items in aiding doctors to acquire more precise information about a patient’s condition. This is just one of several imaginable opportunities for *consumable radios*.

At this time there are essentially two kinds of radio systems: 1) those making use of the electromagnetic spectrum in the traditional way (broadcast, emergency services, military, amateur operators, and the like) *without a fee*; and 2) those involving various sorts of large-scale service providers. Organization and regulation in the first case is implemented solely through national and international agreements, including such bodies as the FCC and ARRL in the United States about how the available spectrum may be utilized. In the second case, while spectral allocations must still conform to such agreements, the day-to-day operation is affected entirely through high-level computer control of every channel, use time on which is *purchased* by the consumer, and for which channel allocations are likewise *purchased*, often by auction. To date, only the second of these markets has been of interest to the SoC manufacturer, since the product volumes are very high (for example, 150-M GSM handsets will be sold this year) and therefore there is a good prospect for profits even at very low prices.

But there is another class of radio devices that may turn out being bigger by volume than even cell-phone transceivers, for which advanced analog expertise will be needed. This is the class of *self-organizing radio systems*. The essential idea here is that rather than depending on a complex, highly structured software-based organization to control the pathways through which signals are transmitted, this task may be taken over by a network of simple radio devices acting autonomously to find and make the best connections. Each transceiver (“node”) acts as the link to other nodes in a potentially large network, making decisions about spectrum utilization within an allocated band. There are many interesting properties of self-organizing automata of this sort, and it is

likely that these will be developed for a wide variety of short-range applications, for example, between many nodes in a room (a home, a clinic, an office) or in a larger building, all needing access to a hub. Certainly, firmware will play an indispensable role in these systems. But by having embedded ID, the data packets will contain unique source and destination tags, as well as information content, and there will be no need for a central controller. As each new node is introduced into the locale, the only consequence may be a small increase in access time (depending on the channel statistics). The design of the frequency plan and the careful control of transmit power levels and receiver intermodulation will remain crucial analog aspects of these systems.

A further new use of radio systems is in the area of RF ID tags. Many ideas have been proposed and developed, and some of these are highly dependent on arcane aspects of physical phenomena. For example, Neil Gershenfeld of MIT's Physics and Media Lab is pursuing multiple resonances in printable cards [44], [45]. The interrogation of these, and reliable extraction of data, will require a whole new set of radio techniques, of a kind never before required, and their development represents one more way in which analog novelty will be critical to the success of the initiative.

Yet another potential growth area is that of "bandwidth arbitrage," services offering information routes which cram data packets into the unused spaces between other types of service occupying a given channel. Certain types of access to and from the Internet will be through devices that are described by Neil Gershenfeld as "bit dribblers." A rather simple example would be the remote monitoring and control of one's home environment. Being sensor rich, there are opportunities here for analog signal conditioning. There will doubtless be numerous other and more important domestic and industrial applications for low-bandwidth routes, at many millions of IPCs, while the demand for high-bandwidth connections will continue to escalate. Looking far over the horizon, we can anticipate that the successful development of quantum computation will significantly depend on new applications for special radio-frequency techniques [46]–[48].

IV. CONCLUSION

Opportunities for gratifying and rewarding careers in analog design abound. Because of the size of the global market, gross revenues for analog components continue to rise, even as the analog percentage of the total dollar volume for electronic components may be declining. It is becoming apparent to the investment community that those companies with proven skills in the design, production, testing, and applications support of analog ICs provide some of the better returns on investment during a time when profit margins for commodity ICs in general are under great pressure. The renewed importance of an "analog emphasis" has not escaped many companies who for years were happy to be known primarily as vendors of digital ICs, but who now seem to go out of their way to capitalize on the word

"analog" by emblazoning it across their advertisements and press releases.

We are not, after all, at the end of the Analog Age, but it is very obvious that neither can we return to a total dependence on analog techniques. Rather, at this millennial milestone, we are at the beginning of a new era characterized by an inescapable symbiosis in semiconductor circuit techniques, in which many formerly analog functions are now more economically and robustly realized in largely digital ways, while those functions that do not lend themselves to a digital implementation continue to provide their unique services alongside large tracts of VLSI. Few of us have the wisdom or vision to state with certainty how this new, synergistic way of using electronics will unfold, or to what new capabilities it will lead.

However, it is safe to say that, in the future, the contentious contrasting of the benefits of analog "versus" DSP will become a thing of the past, as we treat these domains in a more balanced fashion, as *complementary*—rather than *competing* alternatives for ownership of the solution space. It is also safe to predict that many *purely analog* elements will always be needed. Perhaps they will even find large-scale applications in neuronal-based thinking systems. It is just possible that one day, in some far-off age, you will be reading a paper like this about the demise of digital systems, reflecting how, yes, they *were* useful, once, in their time. It is likely that they, and analog systems, are each only one of numerous and yet unimagined ways of having electrons do our bidding.

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Barrie Gilbert (Fellow, IEEE) was with Tektronix from 1964 to 1970, where he worked on sampling and real-time oscilloscopes and designed many of the first integrated circuits. Many classic analog design techniques were invented during this period, including translinear circuits and superintegration, a forerunner of I^2L . From 1970 to 1972, he was a Group Leader at Plessey Research Laboratories, England, addressing optical character recognition (OCR) systems, hand-writing recognition, optical holographic memories, and early semiconductor memories. He joined Analog Devices Inc. in 1972 and has promoted technology initiatives and designed some 50 products. He is currently Director of the Northwest Labs of ADI, Beaverton, OR, developing analog ICs with an emphasis on high-frequency/nonlinear functions. He devotes much of his time to teaching analog design, in short courses and seminars in Europe, Asia and the USA. He has more than 50 issued patents in the field of analog circuits, has authored about 40 papers, and is coauthor of several books.

He has served on several IEEE program committee, is an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, on the Editorial Board of Analog Integrated Circuits and Signal Processing, and a Reviewer for *Electronics Letters*. He received the IEEE "Outstanding Achievement Award" (1970), and the IEEE Solid State Circuits Council "Outstanding Development Award" (1986). He has received the Best Paper Award at the International Solid-State Circuits Conference five times, was "Oregon Researcher of the Year" in 1990, and received the IEEE Solid State Circuits Award (1992) for "Contributions to Nonlinear Signal Processing." He was awarded an Honorary Doctorate of Engineering from Oregon State University in 1997.