

Monolithic Analog READ-ONLY Memory for Character Generation

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Abstract—Two novel circuit techniques are used in a READ-ONLY memory device that produces analog, rather than digital, outputs. One is a compact analog memory element that is able to store a pair of coordinate values; eighty such elements can be placed on a 65×65 mil die. The other is a scanning technique that utilizes a resistive ladder network coupled to an array of common-emitter transistors, having obvious applications in other areas, for example as an analog-digital converting technique.

INTRODUCTION

BINARY READ-ONLY memories are now widely used for CRT character generation, the most popular form using 35 bits per character displayed as a 5×7 dot matrix. More demanding applications use 64 bits per character, displayed as a 7×9 bit matrix, with the spare bit typically used for vertical shift control in the generation of lower-case letters. In either case, separate circuitry is required to generate the latent dot pattern, and the memory output is used to intensify the beam at the appropriate locations. More advanced character-generating systems use the binary data to increment x - and y -axis integrators, thus producing characters formed from a series of continuous strokes. These methods are useful when large symbols must be displayed, but are more complex; typically, 50–100 bits per character are required to produce a high-quality display. Many other methods have been used with varying degrees of success.

The design objectives for the character generator discussed here were unusual in several ways, and available approaches were not sufficient. The solution is novel: a bipolar analog READ-ONLY memory having continuous (rather than digital) outputs that directly drive the x and y inputs of a CRT display device to trace out the character. Although the outputs are in analog form, the programming of each set of characters is by means of the usual oxide-etch mask, and it is possible to regard each 10-character circuit as a 1440-bit READ-ONLY memory with direct D - A conversion integral with the bit-storage elements.

The characters are generated from seven contiguous strokes, each of which may take a large number of possible lengths and angles. This allows considerable freedom in the formation of aesthetically satisfying symbol shapes as Fig. 1 demonstrates. Italics can be

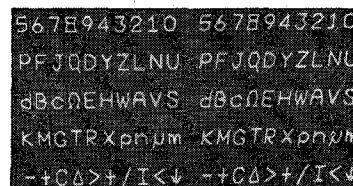


Fig. 1. Typical sets of characters generated by the circuit described. Poor resolution is due to the small symbol per spot-size ratio. Right-hand set was italicized by adding approximately 10 percent of the vertical signal to the horizontal channel.

produced by adding some of the vertical output to the horizontal signal.

Only a 20-V 4-mA supply and a triangular scanning voltage are required to power the circuit, and characters can be formed at any rate from dc to about 10^6 per second. Any number of circuits can be combined to produce larger sets of characters; typically 50 characters are available for a power expenditure of 400 mW. Addressing is not through the usual binary codes, but by a row and column method. Each circuit constitutes a row, and the 10 column-select lines are common to all circuits (Fig. 2). Further, the column-select input is a current in the range from 0 to 1 or 2 mA, and the character display size is directly proportional to this current.

Although well suited to its intended application (a low-cost display system for automatic readout of oscilloscope scale factors) this approach lacks universality. Broken characters (such as $?$, $=$, $;$) are not readily generated, due to the absence of z -axis data within the memory. Also, the intensity of each stroke is inversely proportional to its length, and repeated strokes are of greater intensity. Because of its limited applicability, emphasis will be placed on two basic circuit techniques that are of more general use: 1) a simple READ-ONLY analog memory element that stores a pair of coordinates; and 2) a new circuit technique for steering a current smoothly through an array of transistors.

STROKE REQUIREMENTS

A character is stored as a series of coordinate pairs that are joined by linear segments by the scanning action of the circuit. The total data-storage requirements, and consequently the die size, are directly related to a number of such coordinate pairs, and it is therefore important to use the smallest number of strokes consistent with meeting aesthetic demands. This is, of course, a subjective criterion, but some idea of the dependence of

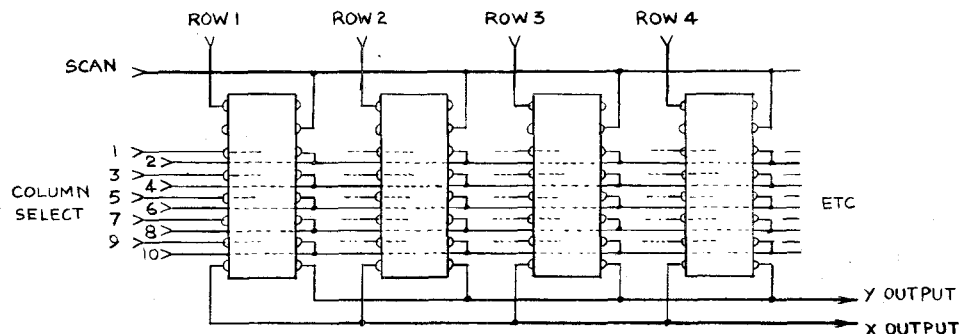


Fig. 2. Characters are arranged in rows of 10, each row corresponding to one integrated circuit. Any number of rows may be combined.

quality as a function of the number of strokes can be gained from Fig. 3. Here the numerals have been constructed using 4–9 strokes, each being allowed unrestricted length and angle. It is apparent that some numerals, for example 1, 4, and 7, gain nothing as the stroke count is increased, whereas others, notably the 8, stubbornly refuse to improve until over 10 strokes are used. The situation is similar with other standard symbols. On the basis of careful studies, seven was chosen as an optimum compromise for the number of strokes.

EARLY COORDINATE GENERATORS

Several methods were considered as a means of storing analog variables in an integrated structure. Some of the earliest circuits made used two-dimensional configurations such as that shown in Fig. 4, where the octagonal collector region is used as a current-splitting medium. The current reaching the four output contacts is related to the position of whichever emitter is injecting, and this in turn was determined by connecting the appropriate emitters to sequenced triangular current sources. This approach is not very flexible and topologically awkward. However, a set of these has been in use in a modified Tektronix 575 curve tracer for about three years with no failures (Fig. 5). A later circuit, shown in Fig. 6, split x - and y -coordinate generators into separate areas on the die, but retained the use of variable-position emitters over a high-resistivity collector. These arrangements allowed infinite resolution of the coordinate locations, but required a special emitter and oxide mask for each set of characters. They also resulted in the outputs being generated across low resistances (the net collector resistance, between the buried-layer contact bars) and this made it difficult to combine several circuits into a matrix.

MULTIEMITTER COORDINATE GENERATOR

The method finally chosen to determine the breakpoint coordinates is shown in Fig. 7(a). An emitter supply current I_E is divided into three components I_x , I_y , and I_z by a trio of transistors Q_x , Q_y , and Q_z . The first two current components correspond to the x and y values of the coordinate, the third represents the unused excess I_E

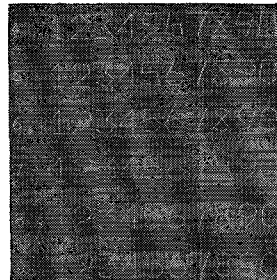


Fig. 3. Illustration of how symbol quality is influenced by the number of strokes. Although only the numerals are shown, few symbols improve beyond seven strokes.

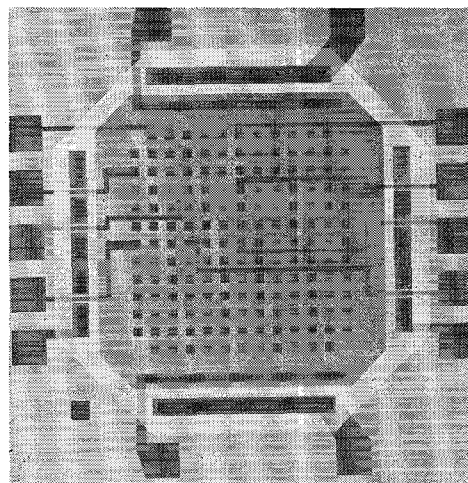


Fig. 4. Early character-generating device. Collector region is of $2\ \Omega\cdot\text{cm}$ n-type material, and forms a current-dividing sheet. Two vertical outputs and two horizontal outputs are taken from the sides of the sheet. Emitter location determines coordinate values.

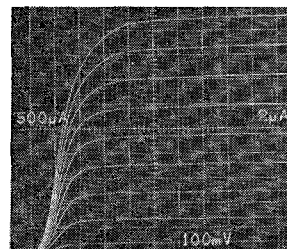


Fig. 5. Typical characters generated by the devices shown in Fig. 4, used here to annotate a curve-tracer display.

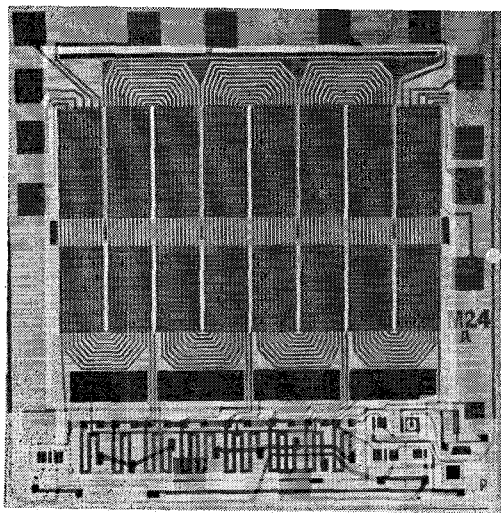


Fig. 6. Later character generator. Here, the x - and y -coordinate regions have been separated, but use is still made of a high-resistivity collector for current division. Emitter locations are infinitely variable, affording an unrestricted range of coordinate values. 60- $\times$ 60-mil die.

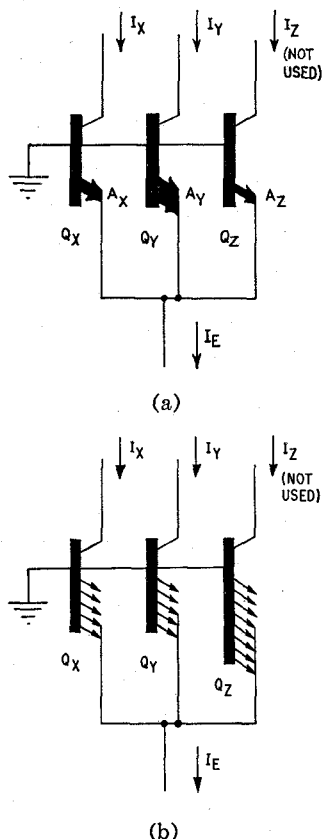


Fig. 7. (a) Final method adopted for coordinate storage. Three transistors share a current source I_E . The collector currents are in the same ratio as the emitter areas. (b) Actual scheme uses multiple-emitter transistors to improve area-ratio accuracy and permit programming by the oxide mask.

$-I_x - I_y$ over that required to produce an arbitrary point.

Because the base-emitter voltages for all three transistors are the same, the emitter-current densities will

also be equal, and consequently the emitter currents are in direct proportion to the emitter-junction area. (This makes the assumption that no current crowding occurs, valid for the low currents used in this application.) Thus, any point for which the sum $I_x + I_y$ is less than I_E may be generated, corresponding to a coordinate plane bounded by the points $(0, 0)$, $(I_E, 0)$, $(0, I_E)$.

To avoid the need to use a special emitter mask for each set of characters, the individual variable-area emitters are replaced by multiple emitters, only some of which are connected through the use of a programmable oxide-etch mask. This also ensures very good area rationing of the emitter junctions [Fig. 7(b)]. However, the coordinates are now limited to points defined by the expressions

$$X = \frac{N_x}{N_x + N_y + N_z}, \quad Y = \frac{N_y}{N_x + N_y + N_z} \quad (1)$$

where N_x , N_y , and N_z are integral. Clearly, the total number of available emitters determines the resolution with which a point may be defined. A study revealed that for character-generating purposes, a total of five emitters in the x and y transistors and eight in the z transistor were adequate.¹ The emitters are identical, 0.4 $\times$ 0.6 mil in size. A further restriction was made that the total connected emitters $N_x + N_y + N_z$ must be between five and ten. The reason for this will become clear when the scanning method is discussed. The points available with these restrictions applied are shown in Fig. 8(a). In this application, some of the points are not used; the character origin is shifted to the point $(0.1, 0.1)$, to provide a below-the-baseline capability and to correctly position the decimal point (which is generated by simply removing the current I_E). These manipulations result in a modified matrix of points, shown in Fig. 8(b). Notice that the peak amplitude of the output currents is 40 percent of I_E in either a vertical or horizontal direction. Although the limited number of available coordinates might seem to impose unacceptable constraints on the appearance of the symbols, the set shown in Fig. 1 was produced with this matrix, and demonstrates that adequate freedom of form is available.

The advantages of the multiple-emitter coordinate generator as an analog READ-ONLY memory element are the following.

1) Efficient area utilization; only two collector regions are needed for the x and y outputs of an entire generator (the I_z output is sunk directly into the bulk epitaxial layer tied to the $V+$ supply). Also there are only a few common base regions, as will become apparent.

¹ Some thought was given to using emitter areas having a BCD weighting, but the area required in this case would have been unnecessarily great. Note that since 18 individual emitters are available for programming, the coordinate generator could be regarded as an 18-bit ROM subunit. However, less than 2^{18} different combinations are possible; that is, the coding efficiency is less than maximum.

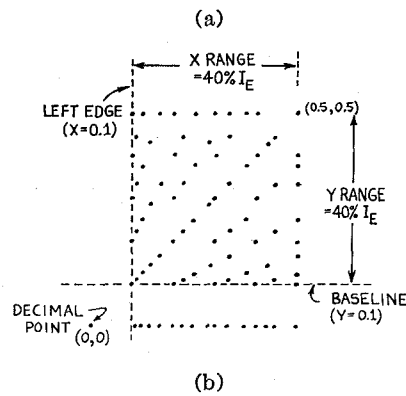
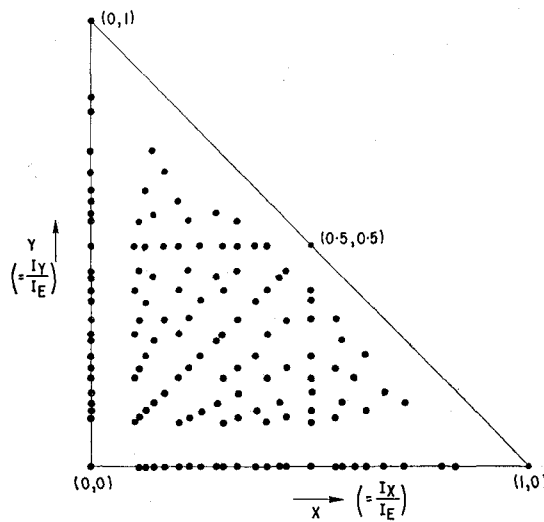


Fig. 8. (a) Range of possible coordinates for $N_{x(\text{MAX})} = N_{y(\text{MAX})} = 5$ and $N_{x(\text{MAX})} = 8$. (b) Modified matrix uses the line $x = 0.1$ for a baseline to provide below-the-line capability.

- 2) Ease of combining outputs from several generators; the outputs appear from "free" collectors.
- 3) Control of scale; character size is directly proportional to I_E .
- 4) Temperature immunity; only the ratios of emitter areas determine the coordinate locations.
- 5) Easily programmed by the oxide-etch mask.

DEVELOPMENT OF THE COMPLETE MEMORY

Having described the basic coordinate-defining element, the organization of a 10-character generator will now be developed. First, eight coordinate elements are connected as shown in Fig. 9. The numbers of connected emitters correspond to the figure "3". All emitters in this group are connected together to an input pad that selects the corresponding character. The eight base connections are common to all 10 of the character-generating groups as in Fig. 9. This is readily seen by referring to the circuit layout shown in Fig. 10. The die is divided into two halves, each storing five characters, and each having common collector regions for the x and y outputs. Into each of these collector regions are diffused eight base regions, each in turn containing 25 emitters. Eight common base regions are also diffused into the

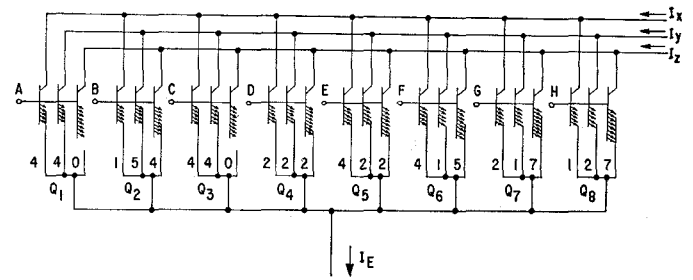


Fig. 9. A group of eight transistor trios is needed to define the eight coordinate pairs of a character. Bases connect to the scanning network. Three collector regions are common to the entire generator.

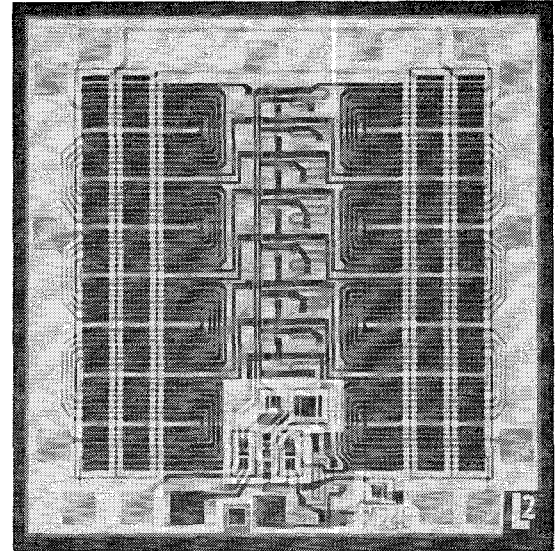


Fig. 10. Mask layout for the complete generator. Characters are grouped into two sets of five. Scanning network occupies the center region, and remaining circuitry is for chip select and the scan buffer-amplifier. Outputs are taken directly from the collectors of the coordinate transistors.

bulk epitaxial layer to form the Q_z transistors, and these each contain 40 emitters. Corresponding emitters for each character are connected to input pads by the metalization. The die size is 65×65 mils.

A network of resistors in the center of the die layout can be seen. Its purpose will now be explained.

SCANNING BY MEANS OF A RESISTIVE LADDER

If a ring counter or shift register had been connected to the eight bases of a character-generating group in order to scan the coordinates, only a series of dots could be generated. A method is required that permits the emitter current I_E to be scanned smoothly from one coordinate trio to the next. There are several ways to achieve this; a resistive ladder network is the simplest.

Consider first the situation depicted in Fig. 11. Eight simple transistors (representing the trios of transistors actually used) connected to a resistor network are shown. If the restriction on the total number of connected emitters has been observed, the emitter areas of these eight

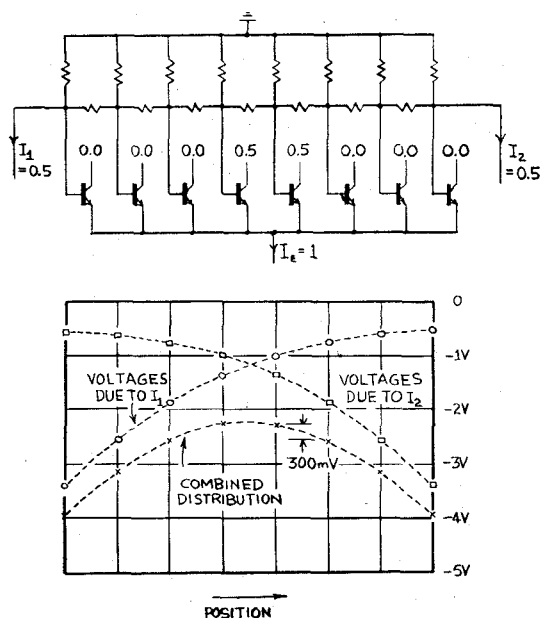


Fig. 11. Scanning network is simply a resistive-ladder network. When biased as shown, there is a point of maximum potential at the center of the network. Consequently, the two center transistors conduct I_E .

transistors can be assumed equal. Small departures from this condition do not affect seriously the operation or the analysis.

At this point, a somewhat intuitive discussion will be used, to make the simplicity of the scanning mechanism clear. A more rigorous analysis is given in Appendix I. The ladder bias currents in Fig. 11 are of such a polarity as to pull down the voltage on the ends of the network. I_1 sets up a series of voltages on the eight nodes that diminish from left to right, and I_2 causes a similar voltage distribution from right to left. When $I_1 = I_2$, the combined voltage distribution shows a maximum at the center of the network. Actually, because there are an even number of nodes, the two middle transistors have the same base voltage, and their emitter currents are therefore equal. Also, the two adjacent transistors have base voltages 300 mV (in this typical case) less than the center pair. Therefore, these are virtually cut off, and receive very little of the emitter supply current I_E . To be exact, the emitter current of each transistor is simply shown to be

$$I_n = \frac{\exp [qV_n/KT]}{\sum_{n=1}^8 \exp [qV_n/KT]} \quad (2)$$

where the suffix n refers to a specific node and its associated transistor. With the voltages shown in Fig. 11, over 99.99 percent of I_E flows into the center pair of transistors. The outputs from the generator, therefore, correspond to a point halfway between the points defined by the two center transistors (remembering that each of the transistors in Fig. 11 corresponds to a multiemitter

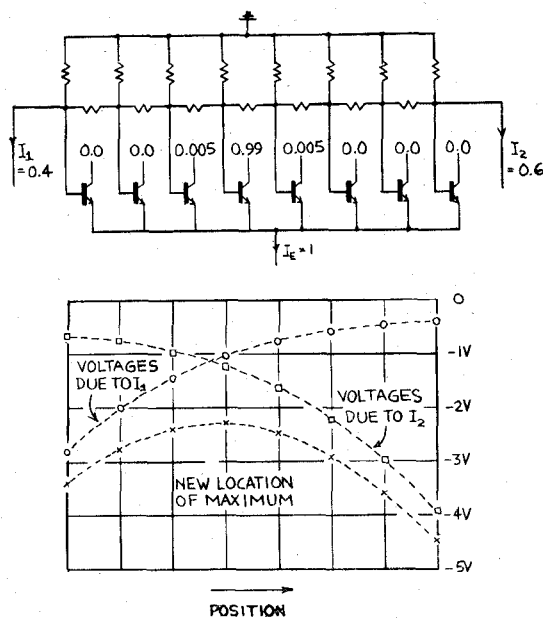


Fig. 12. When the bias is unbalanced, maximum potential point shifts to the left or right, causing each of the transistors in the array to conduct for a brief period.

current-dividing trio of transistors such as in Fig. 7).

If the bias currents to the ladder network are now changed, the voltage distribution will no longer be symmetrical and the maximum will shift its position. It is this that makes the ladder network so useful when coupled to an array of common-emitter transistors. A potential maximum can be moved from left to right under the control of the bias currents, and the current I_E will be steered into the transistor whose base is most positive (for the n-p-n transistors shown). If the interpolated maximum occurs between transistors, an effective transistor can be imagined having proportional parts of two or more sets of coordinates. Notice that the location of the maximum is independent of the magnitude of the total bias current; only the ratio of currents is important.

Thus, in Fig. 12, the left-hand bias current is shown as 0.4 units, whereas the right-hand current is now 0.6 units (a differential current drive is assumed). Under these bias conditions the potential maximum occurs at the fourth transistor, which therefore receives the majority of I_E , and the coordinate is now defined almost entirely by this transistor (trio). If this change in bias conditions had been brought about gradually, the result on the display would have been a partial stroke. By gradually raising I_1 from zero to its full value while reducing I_2 in a complementary manner, the maximum can be made to sweep across the full set of eight coordinate-defining transistors, and the entire character will be generated as a series of strokes.

In order to achieve the correct scanning conditions for character generation, the current in any one coordinate trio should be linearly increasing with time as

that in an adjacent trio is decreasing, with the further requirement that only two trios are active simultaneously. Additionally, the time spent in generating each stroke should be the same,² or, if the ladder drive currents are triangular in waveform, the maximum must move linearly with respect to the bias.

Neither of these conditions is met by a simple repetitive ladder network (all shunt resistances equal, all series resistances equal). However, the requirement of linear motion of the maximum can be closely approximated in several ways, discussed in Appendix I. One of these methods is the use of a parabolic network. Fig. 13 shows the peak region of the voltage distribution curve (normalized to the peak) as a function of bias for such a network, the values for which are given in Fig. 14. Using this network, the variation of each of the eight trio currents was computed to be as shown in Fig. 15(a), and verified experimentally as shown in Fig. 15(b). The requirements calling for linear variation of emitter currents and no more than two transistors active at a time can not be met perfectly by a resistive network due to the exponential characteristics of (2) combined with the linear voltage variations in the network. Note that the argument of the exponents in (2), that is qV_n/KT , is a function of absolute temperature and the absolute magnitude of the ladder bias current. Neither of these dependencies gives rise to any difficulties in practice, but a correction could be made by causing the bias current to be proportional to temperature.

It was mentioned earlier that the total number of connected emitters in the trios should be approximately the same. It should be clear that departures from this condition are accounted for by modifying (2) to read

$$I_n = \frac{A_n \exp [qV_n/KT]}{\sum_{n=1}^8 A_n \exp [qV_n/KT]} \quad (2a)$$

where A_n is the total emitter area of each trio. The consequence of nonequal areas is to increase the dwell time on those coordinates having greater emitter areas and thus produce strokes of uneven intensity.

COMPLETE SCANNING CIRCUITRY

In addition to the memory and ladder network, each die contains a ladder-driver circuit and the associated chip-enable provisions. These are shown in Fig. 14. Q1 and Q2 form a linear amplifier that converts the scan voltage into a pair of complementary currents whose sum is defined by $R2$. The lower limit of the scan voltage is defined by the zener diode D1, and the upper limit by R1. The relatively high input impedance of this stage facilitates the operation of several generators from a common scanning voltage.

² This assumes equal stroke lengths and is desirable to maintain a constant display intensity. In a practical scheme, it is not possible to assume the strokes to be equal, but neither is it practical to use a special ladder for each character as a means of equalizing stroke intensities.

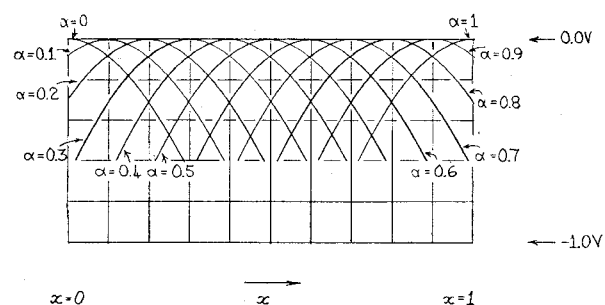


Fig. 13. Motion of the region near the maximum as the bias ratio is varied, for a parabolic ladder network (Appendix I).

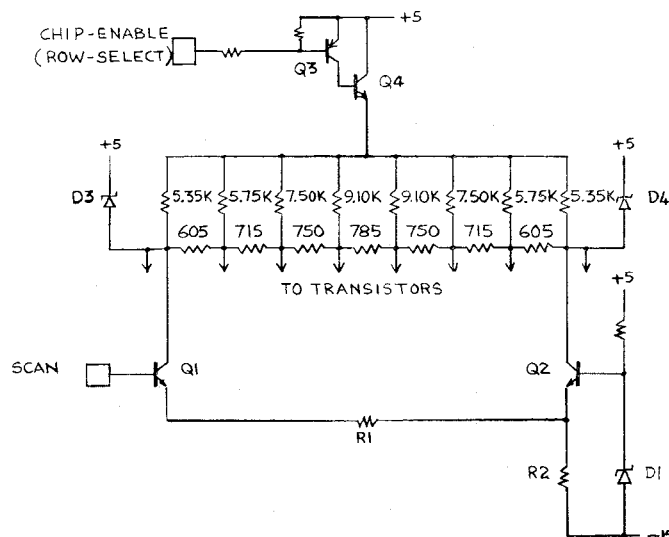
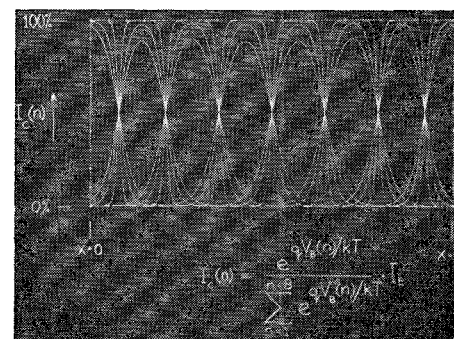
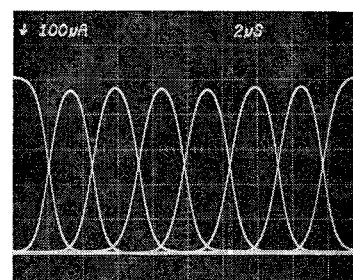


Fig. 14. Complete ladder network and drive circuitry.



(a)



(b)

Fig. 15. Computed (a) and practical (b) curves showing the current in each of the eight transistors as the scanning input is varied over the full range. In the set of computed curves, effects of temperature or bias-current changes are shown.

The chip-enable or row-select input operates to raise or lower the overall ladder potential, thus steering the column-select current (I_E in the previous discussions) into the appropriate package (see also Fig. 2). The input interfaces with collectors of n-p-n transistors in another integrated circuit. These collectors are either nonconducting or saturated to ground. When off, the pull-up transistors Q3 and Q4 are also off, and the ladder network is uniformly at -1.5 V, defined by the zener catching diodes D3 and D4. When selected, Q3 and Q4 pull the ladder network up sufficiently to prevent either D3 or D4 from conducting, and the variable-position potential maximum can be established.

CONCLUSION

An analog READ-ONLY memory has been developed for use as a character generator, but also has applications as a general-purpose function generator. It has the advantage of requiring only a 20-V power supply and a scanning voltage to operate directly into a CRT display. Two techniques are used that appear to be of general use: 1) the technique of current division by means of multiple-emitter transistors, and 2) the technique of steering a current into one of several transistors under the control of an analog input through the use of a resistive ladder network. A more complete analysis of the scanning network is presented in Appendix I. Appendix II outlines an improved scanning method, using nonlinear ladder elements.

APPENDIX I

OPTIMIZATION OF THE SCANNING NETWORK

The purpose of this section is to provide a better understanding of the scanning circuit, which makes use of a resistive ladder network, and show how it can be optimized.

Constant-Attenuation Ladder

Consider first a finite resistive ladder network made up of N identical L sections, as shown in Fig. 16. Such a ladder has an asymptotic impedance of

$$Z = (1 - \lambda)R \quad (3)$$

where

$$\lambda = 1 - \frac{\sqrt{\mu(\mu + 4)} - \mu}{2} \quad (4)$$

is the voltage attenuation ratio per stage $= [V(x + \Delta x)]/V(x)$ when driven from the left-hand side.

If the network is terminated at each end with this resistance,³ and we assume a large number of sections, it will behave as a portion of an infinite network. Specifically, the voltage distributions along it may be de-

³ Shown in Fig. 16 as made up of two resistances, R and $(1 - \lambda)R/\lambda$.

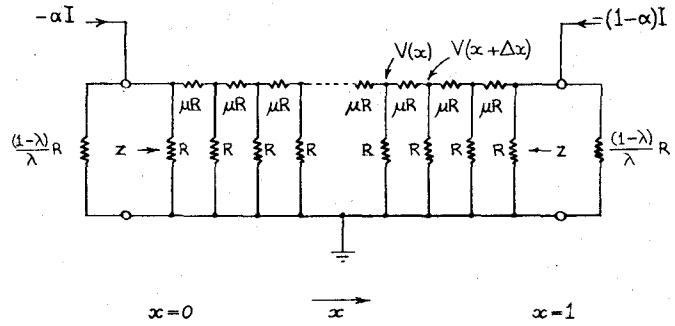


Fig. 16. Simple recursive ladder network.

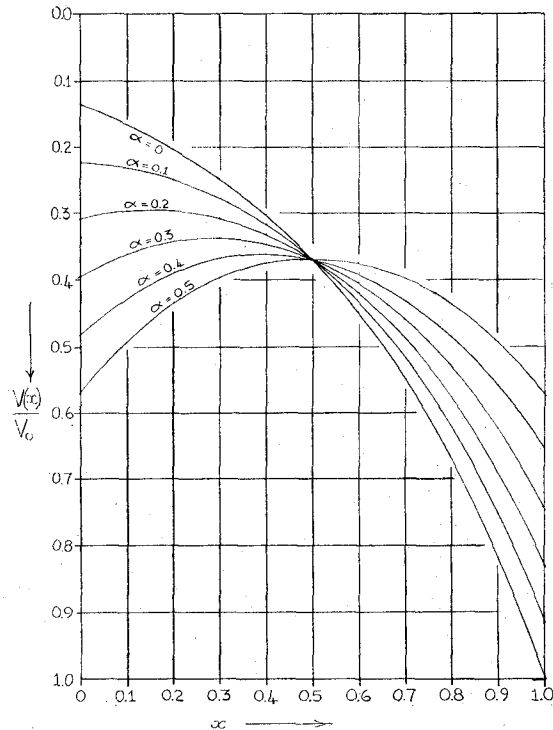


Fig. 17. Typical voltage distributions along the nodes for various values of the bias factor α .

scribed in simple exponential terms. At one end, a current $-\alpha I$ is applied (where $0 > \alpha > 1$) that generates a voltage at this input (the negative sign being introduced to produce a maximum, rather than minimum, potential point). At the other end, a current equal to the complement of the first current, that is $-(1 - \alpha)I$, is applied. The resulting voltage distribution can be described as the sum of two exponentials.

$$V(x) = V_0 \{ \alpha \exp[-kx] + (1 - \alpha) \exp[-k(1 - x)] \} \quad (5)$$

where $V_0 = -(1 - \lambda)/(1 + \lambda) IR$ is the full-scale input voltage, x is the fractional distance from the input driven by αI ($0 > x > 1$), and k is the attenuation constant $= -N \ln \lambda$.

Typical distributions for the case where $k = 2$ are shown in Fig. 17. Note in passing that the common point of intersection is at $V_0 \exp[-k/2]$ and that for small

attenuation constants the voltage distribution for the balanced condition approximates to a simple parabolic form:

$$V(x) \simeq V_0[1 - (k^2/2) \times (1 - x)], \quad k < 1, \quad \alpha = \frac{1}{2}. \quad (6)$$

In general, we want to determine the location and magnitude of the maximum potential point and the field gradient at that point, for any value of the bias ratio α . By differentiation of (5) the maximum is found to occur at

$$x \Big|_{V=\text{MAX}} = \frac{1}{2} \left[1 + \frac{1}{k} \ln \frac{\alpha}{1-\alpha} \right] \quad (7)$$

and by substituting this value of x into (5) we find

$$V_{\text{MAX}} = \frac{2V_0}{\exp[k/2]} \sqrt{\alpha(1-\alpha)}. \quad (8)$$

The field gradient is given by

$$\begin{aligned} (dE/dx) &= (d^2V/dx^2) \\ &= V_0 \{ \alpha k^2 \exp[-kx] + (1-\alpha)k^2 \exp[-k(1-x)] \} \\ &= k^2 V(x) \end{aligned} \quad (9)$$

$$= \frac{2k^2 V_0}{\exp[k/2]} \sqrt{\alpha(1-\alpha)} \quad \text{at the maximum.} \quad (10)$$

The importance of the field gradient will be seen in a moment. At this point, some observations can be made.

1) The maximum does not move linearly with respect to the bias ratio α , but to a $\ln(\alpha/1-\alpha)$ law as depicted in Fig. 18 for $k = 1, 2, 4$.

2) The voltage and field gradient at the maximum point are not constant, but vary according to a $\sqrt{\alpha(1-\alpha)}$ law.

3) If the attenuation ratio k is too large, the maximum is very broad and barely moves from the midpoint of the network as the bias is varied. If too small, the voltage distribution becomes almost a straight line between the two inputs, and there is again a broad maximum; however, in this case the location is a sensitive function of bias. Fig. 19 shows the voltage distributions for several values of k and $\alpha = 0.5$. Note also that (10) indicates the field gradient is greatest when $k = 4$.

The physical significance of these characteristics is as follows.

1) Since the maximum does not move linearly, the strokes will not be evenly spaced in time if a linear ramp is used to scan the character.

2) The fact that the absolute value of the voltage at the maximum varies, leads to problems at high scanning rates. Associated with the drive lines to the emitters of the character-generating trios are capacitances that must charge and discharge as the emitters follow the maximum. The resulting displacement current causes the character to become slightly smaller during the first half of the scan (as V_{MAX} falls, current is subtracted from the

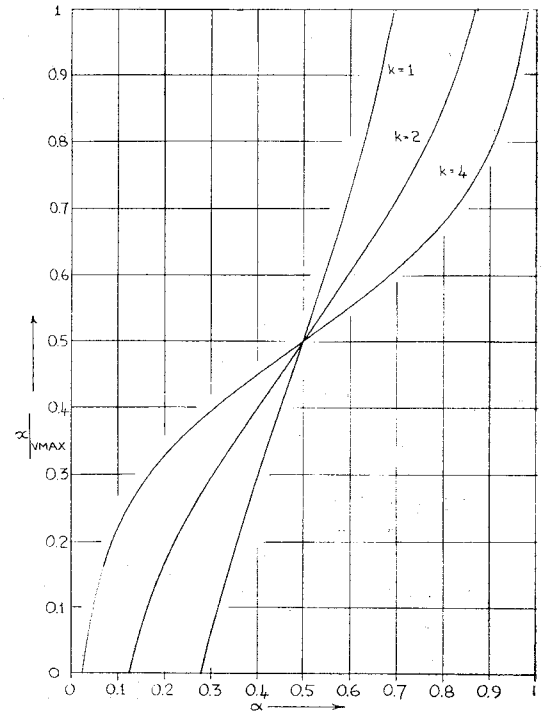


Fig. 18. Locus of the maximum as a function of α with k as parameter.

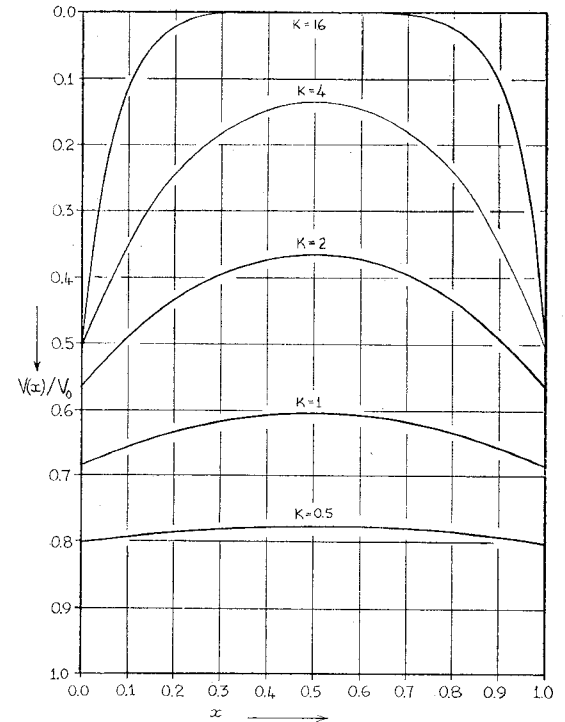


Fig. 19. Voltage distributions for $\alpha = 0.5$ and various values of k .

column current) and enlarge during the second half, thus distorting the character.

3) The field gradient determines how sharp the selection of one trio out of all the rest will be. If too large, the transition from one trio to the next will be abrupt, and the character will dwell at the break points. If too small, full selection of each coordinate will not be

achieved. Because the gradient is critical, variations such as described by (10) can not be tolerated.

Satisfying the Scanning Requirements

It would seem possible to find a simple resistive network able to produce simultaneously a linear motion of the maximum and maintain both a constant voltage and a constant field gradient at the maximum. However, this is not so, as will be seen.

The linear-motion requirements can be met in several ways. One interesting possibility is to note that the $\ln(\alpha/1 - \alpha)$ relationship between the location of V_{MAX} and α is the exact inverse of the relationship between collector currents in a differential-transistor amplifier (with no emitter resistors) and the differential base voltage input to this amplifier. (Turn Fig. 18 sidewise to see this.) The temperature dependence of the transistor amplifier can be readily compensated. This method provides the required linear motion even when k is optimized to produce the highest field gradient. Unfortunately, the variation in the voltage and gradient at the peak is unacceptable.

A second approach is to note that when k is small, the maximum does move almost linearly. By solving (7) for α , the values required to scan from $x = 0$ to $x = 1$ are, respectively,

$$\alpha_0 = [1 + \exp(-k)]^{-1}$$

and

$$\alpha_1 = [1 + \exp(k)]^{-1} = 1 - \alpha_0. \quad (11)$$

For example, when $k = 1$, the maximum moves the full length of the network for $\alpha = 0.27$ to $\alpha = 0.73$. Furthermore, the voltage and field gradient at the maximum vary only 11.2 percent over this range. Therefore, this would appear to be a good solution. However, it should be noted that to maintain the necessary field gradient, the bias currents must be increased, and although the percentage variation in the voltage at the maximum decreases, the absolute value increases as k becomes smaller. It readily can be shown that the absolute variation in V_{MAX} is given by

$$\Delta V_{\text{MAX}} = \frac{2V_0}{\exp[k/2]} \left[\frac{1}{2} - \frac{\exp[k/2]}{1 + \exp[k]} \right] \quad (12)$$

$$\propto (1/K^2) \left[\frac{1}{2} - \frac{\exp[k/2]}{1 + \exp[k]} \right], \quad (d^2V/dx^2). \quad (13)$$

By intuitive reasoning, we can reach the conclusion that V_{MAX} can never be constant for the case where the network is driven symmetrically, since only the midpoint remains fixed. For now, we will have to be content with satisfying the conditions of linear scan and constant field gradient. Later, a solution to this problem will be presented.

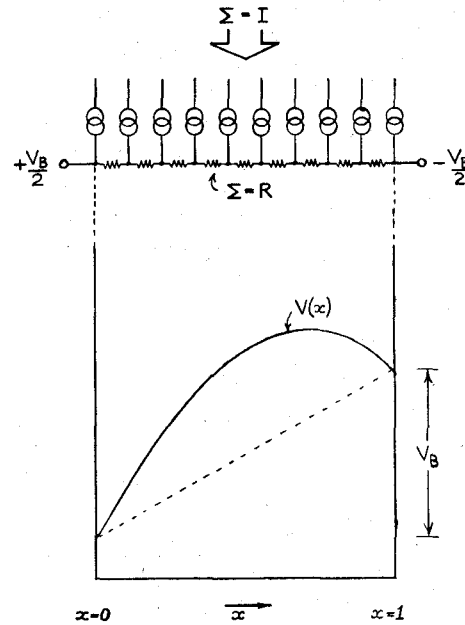


Fig. 20. Network using current sources and resistors. In this case, $V(x)$ is the sum of a parabolic and linear distribution, and the position of the maximum is linearly dependent on V_B .

Network Using Current Sources

The fact that the behavior becomes more linear as k is reduced suggests a third solution, make $k = 0$. In this limiting case, the shunt resistors are infinite, that is, they are identical current sources, and the voltage distribution along the nodes is perfectly parabolic for the balanced condition. We now use complementary bias voltage $\pm V_B/2$ to drive the ends of the network; these effectively introduce a slope additively to the parabolic distribution (Fig. 20). Thus, the voltage distribution is of the form

$$V(x) = (IR/2) \times (1 - x) + V_B(x - \frac{1}{2}) \quad (14)$$

where I is the sum of all the current sources, R is the total resistance of the series elements, and $0 < x < 1$ (again, taking a network of unit length).

The maximum value of this expression occurs at

$$X|_{\text{MAX}} = \frac{1}{2} + (V_B/IR). \quad (15)$$

This simple expression shows that the maximum is linearly dependent on V_B and that full motion occurs for $V_B = \pm IR/2$. Also, the field gradient is constant everywhere.

$$(d^2V/dx^2) = IR \text{ per unit length squared.} \quad (16)$$

This would appear to be the ideal situation, but recall that V_{MAX} can not be constant for the drive conditions stated. In fact

$$V_{\text{MAX}} = \frac{1}{2}[(V_B/IR) + (IR/4)] \quad (17)$$

and the variation in the quantity between $V_B = 0$ and $V_B = \pm IR/2$ is $IR/8$.

Another possible disadvantage is that we must use ac-

tive current sources, and the drive voltage must now be accurately ratioed to these currents.

Parabolic Network

Since the parabolic voltage distribution is the only one meeting the required condition of constant field gradient, it is reasonable to ask whether a passive network could be constructed to produce this kind of distribution. If so, it would satisfy most of the requirements and avoid the need for active current sources.

This was the solution adopted in the character generator. The network is identical in form to that shown in Fig. 16, but the resistor values are tapered to produce the functions

$$f(x) = p + x^2(1 - p),$$

driven from right-hand side (18a)

$$f(1 - x) = p + (1 - x)^2(1 - p),$$

driven from left-hand side (18b)

where p is the fractional voltage appearing at one end of the network due to an input at the other end. This allows for the fact that the ends are current driven.

In general, therefore,

$$(V(x)/V_0) = \alpha[p + x^2(1 - p)] + (1 - \alpha)[p + (1 - x)^2(1 - p)] \quad (19)$$

where α is the bias ratio, previously defined, and V_0 is the full-scale input voltage (a negative quantity). This reduces to

$$(V(x)/V_0) = (1 - p)[x^2 - 2\alpha x + \alpha] + p. \quad (20)$$

The maximum thus occurs

$$x = \alpha \quad (21)$$

and the field gradient is constant and equal to

$$(d^2V(x)/dx^2) = 2V_0(1 - p) \text{ per unit length squared.} \quad (22)$$

Methods to Maintain Constant V_{MAX}

It is possible to add active circuitry to keep V_{MAX} constant. One method is to introduce a common-mode variation in drive currents or voltages, to compensate in an open-loop fashion for variations in V_{MAX} . A better solution is to sense V_{MAX} and hold it constant by a feedback circuit. The emitters of the scanned transistors can be used as a sensing point, although in the character-generator case an extra set of transistors must be included for this purpose, since there are many emitter lines, only one of which is driven.

It should be remembered that these variations are of concern only when high-speed operation ($>10^5$ symbols/s) of a large set of generators is required.

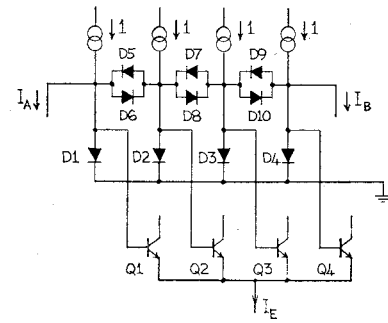


Fig. 21. Nonlinear network of diodes and current sources provides a means for linearly positioning the current and produces perfectly triangular current pulses in the transistors.

APPENDIX II

SCANNING NETWORK USING NONLINEAR ELEMENTS

A second-generation scanning network has been developed that has superior characteristics to the purely resistive network. In particular, the emitter potential of the scanned transistors remains constant (even over a wide temperature range) and, more importantly, the current pulses in the scanned transistors are now precisely triangular. This has obvious advantages in the character-generating application since the strokes are now of constant intensity along their length and break sharply at the coordinates. This also opens up applications in the area of precise function generation using monolithic analog READ-ONLY memories.

The basic idea is presented in Fig. 21, which shows a four-section network for simplicity. The four scanned transistors $Q1-Q4$ are assumed to have equal emitter area.⁴ The four diodes $D1-D4$ are likewise assumed to have equal junction areas, and would, in practice, be transistors connected as diodes. The remaining diodes $D5-D10$ are not critical, but low-voltage devices such as Al-Si Schottky diodes are preferable. The four current sources are identical, and Fig. 21 shows them as having unit magnitude. The scanning drive is a pair of complementary currents I_A and I_B whose sum is always one unit less than the sum of the current sources; in this case, the drive currents must have a total magnitude of three units.

The operation is simple. Assume first that $I_A = 0$, $I_B = 3$. To satisfy these conditions, the last three current sources must add up to I_B , and thus $D8$ and $D10$ are forward biased. Also, all of the current in source number 1 flows in $D1$. Now, the current densities in the emitters of $Q1-Q4$ must be the same as those in $D1-D4$, and since only $D1$ is conducting at this time, all of I_E flows in the emitter of $Q1$.

Now put $I_A = 0.5$, $I_B = 2.5$. A similar consideration of

⁴For the case where this is not so, see B. Gilbert, "A new wideband amplifier technique," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 353-365, December 1968.

where all the currents go shows that $D3$ and $D4$ are still nonconducting, and $D1$ and $D2$ each conduct 0.5 mA . Therefore, I_E divides equally between $Q1$ and $Q2$. If we had chosen $I_A = 0.3$, $I_B = 2.7$, the ratio of the currents in $Q1$ and $Q2$ would have been $0.7 I_E$ and $0.3 I_E$, respectively. In other words, there is a linear transference of I_E from $Q1$ to $Q2$ as I_A is increased and I_B reduced. By inserting further typical values, it will seem that, one by one, successive transistors conduct I_E , the transference from one to the next always being linear. Furthermore, the emitter potential of $Q1$ - $Q4$ remains constant, at ground potential if I_E is one unit, never more than a few tens of millivolts away for other values of I_E .

The advantage of using low-voltage diodes for $D5$ - $D10$ is apparent when the potentials at the end of the network are considered. For an N -stage network, the in-

puts will fall to $V_P - (N - 2) V_S$, where V_P is the forward voltage of the shunt diodes and V_S is the forward voltage of the series diodes (note that the diodes $D6$ and $D9$ are zero biased at the ends of the scan, and can actually be omitted). Thus, in an 8-stage character-scanning application, the minimum voltage at the drive terminals is about -1.7 V , which compares very favorably with the resistive network. Notice also that the limiting number of stages is reached when this voltage equals the emitter breakdown of the transistors. Taking this as about 7 V , about 17 stages can be used.

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Correspondence

Nonlinear JFET Model for Computer-Aided Circuit Analysis

Abstract—A simplified circuit model is proposed to represent the nonlinear dc and low-frequency small-signal operation of JFETs. This model is particularly useful for computer-aided circuit analysis programs, such as the iterative nodal analysis program BIAS-3. Operation in the off, resistance, and pinch-off regions of the JFET is included.

IDEAL I-V REPRESENTATION

In Fig. 1, a typical output characteristic (I_D versus V_{DS}) for an n-channel junction field-effect transistor (JFET) is shown. For normal operation, within the first quadrant, the three regions of interest are the cutoff, resistance, and pinch-off regions. The drain current in each region, on the basis of a first-order idealized situation, is

$$I_D = 0 \quad V_{GS} - V_p < 0 \quad (1)$$

$$I_D = \frac{I_{DSS}}{V_p^2} [2(V_{GS} - V_p)V_{DS} - V_{DS}^2] \quad 0 < V_{DS} < V_{GS} - V_p \quad (2)$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad 0 < V_{GS} - V_p < V_{DS} \quad (3)$$

where I_{DSS} and V_p are constants [1], [2] usually determined empirically. The boundary between the resistance and pinch-off

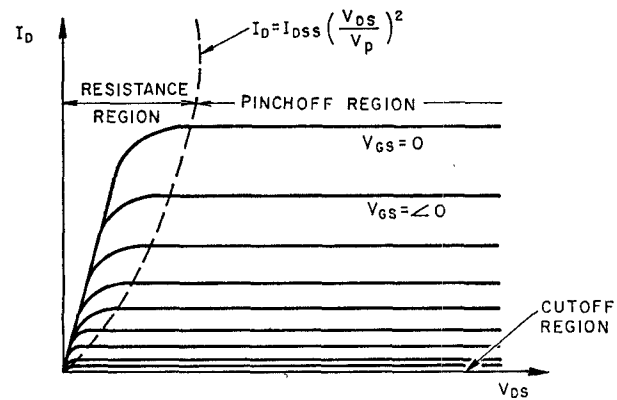


Fig. 1. JFET characteristic curves.

regions is given by

$$I_D = I_{DSS} \left(\frac{V_{DS}}{V_p}\right)^2 \quad (4)$$

For all three regions, the input port is described by

$$I_G = I_{GSS} [\exp(qV_{GS}/kT) - 1] \quad (5)$$

where I_{GSS} is a constant. For normal operation, $V_{GS} \leq 0$ for an n-channel device.

CIRCUIT MODEL IN THE RESISTANCE REGION

The drain current I_D for the resistance region is given by (2). The equation can be expanded in a Taylor series about an operating point V_{DS0} , V_{DS0} . If only first-order terms are retained