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A High-Performance Monolithic Multiplier Using Active Feedback

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Abstract—Since its conception in 1967, the linearized transconductance multiplier (LTM) has rapidly gained acceptance as the preferred approach to the realization of monolithic analog multipliers, and its simplicity has commended it for use in low-cost modular designs. Accuracies of these units have been limited to about 0.5 to 2 percent, and drift and noise performance have generally been worse than that possible using the dominant alternative technique of pulse-width-height modulation. This paper shows that when careful attention is given to all the sources of error it is possible to attain a five-fold improvement in accuracy and corresponding reductions in the drift and noise levels. Odd-order nonlinearities can be reduced to negligible magnitudes by the use of active feedback, by substituting the usual resistive-bridge feedback path by an amplifier identical to that used as the input stages.

I. INTRODUCTION

THE LINEARIZED transconductance multiplier (LTM) technique¹ is now widely used in one or another of its several forms, the commonest of which are shown in Fig. 1. Using ideal transistors these circuits are fundamentally exact and insensitive to isothermal variations of temperature. Compared to alternative multiplication techniques, the LTM core is extremely simple and has intrinsically wide bandwidth. It is the basis of many other "functional" circuits, such

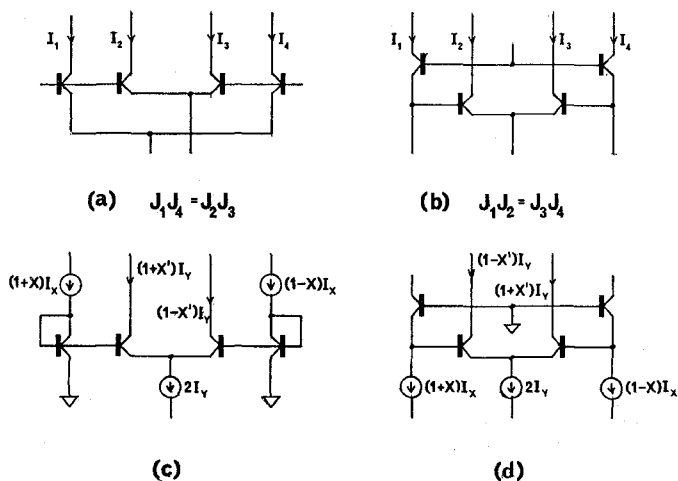


Fig. 1. Basic LTM configurations. (a) "Normal" form. (b) "Inverted" form. (c) Specific version of the normal form having low beta-sensitivity. (d) Common inverted form, which is convenient but has high beta-sensitivity.

as precise two-quadrant dividers, rms converters, vector sum modules, etc.

This paper describes a four-quadrant multiplier designed to make full use of the potential accuracy afforded by this technique using currently available monolithic processes. The basic error sources are reviewed, and methods presented to minimize their effects. A significant improvement has resulted from the use of an active feedback scheme which largely eliminates the nonlinearities introduced by the input amplifiers. Apart from this, the resulting design is similar to most transconductance

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¹ B. Gilbert, "A new wide-band amplifier technique," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 353-365, Dec. 1968.

multipliers. The high performance is a result of the systematic elimination of individual sources of inaccuracy, through careful choice of operating conditions, the use of beta-compensation, and a precise layout. Accuracies of ± 0.1 percent over all four quadrants have been measured on the best prototype devices. This has previously only been possible using the classical precision techniques such as pulse modulation.

II. DESIGN OBJECTIVES

Completely self-contained monolithic circuits performing multiplication, division, squaring, square-rooting (MDSSR) functions have been available for over three years. They are fabricated using a high-quality bipolar process incorporating on-chip thin-film resistors. Accuracies² of better than ± 1 percent can be consistently achieved from fully-trimmed units, and selected units have guaranteed accuracies of ± 0.5 percent. Recently, laser-trimmed versions of these circuits have become available, relieving the user from the need to apply rather tedious trimming procedures to each unit.

However, this accuracy is usually not maintained over a wide temperature or supply-voltage range. A representative device has an accuracy specification of ± 4 percent over the range -55 to $+125^\circ\text{C}$. In fact, even premium-grade modular multipliers using pulse modulation have accuracy-versus-temperature specifications of typically 0.01 percent/ $^\circ\text{C}$.

A new design was therefore conceived whose primary objectives were as follows.

1) To retain the familiar MDSSR format (a complete, calibrated system with fully-stabilized reference voltage and a high-gain output op amp with uncommitted output connection) having the standard interface levels of $\pm 10\text{-V FS}$ with $\pm 15\text{-V}$ supplies.

2) Achieve a high production yield to ± 0.25 percent accuracy at 25°C after nulling offset and scale errors (using an active-circuit laser-trimming technology).

3) Achieve a reliable yield-fraction to ± 0.1 percent trimmed accuracy.

4) Maintain an accuracy of ± 1 percent over the entire -55 to $+125^\circ\text{C}$ range.

5) Reduce supply-related errors to negligible proportions over the range ± 10 to $\pm 20\text{ V}$.

Thus, the primary objectives were intended to fill the need for a high-accuracy "computing" element. Multipliers are often used, of course, in applications where absolute accuracy is of less importance, and consequently the secondary objectives took into account these other requirements.

6) High linearity. With proper design, errors can be held to very low levels, particularly on the Y input, for which the objective was < 0.05 percent nonlinearity.

7) Low noise and drift. This necessitates using as

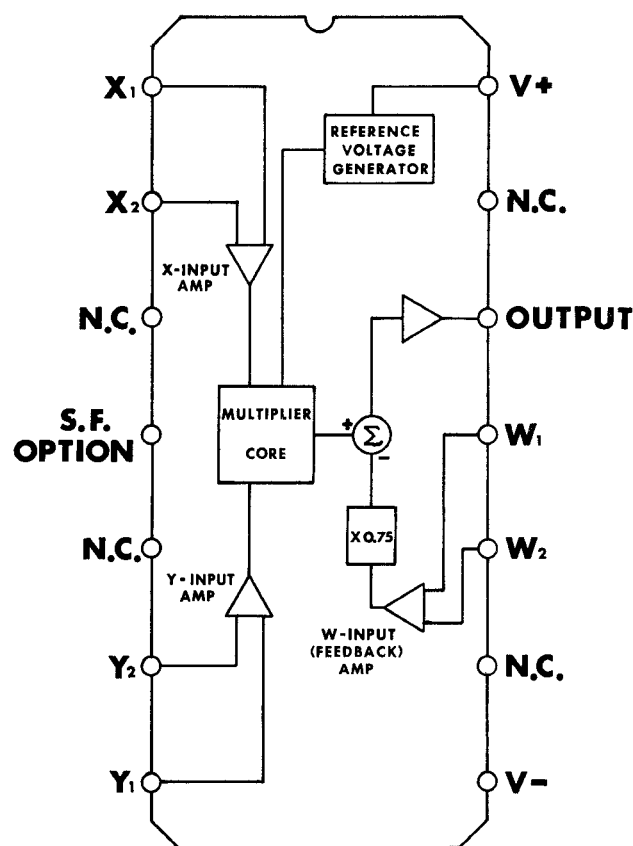


Fig. 2. Package layout of the multiplier described in this paper.

much of the inherent dynamic range of the core as possible, and is thus in conflict with the previous goal.

8) Good dynamics. As a multiplier, the -3 dBs bandwidth should be at least 1 MHz , and the slew rate greater than $25\text{ V}/\mu\text{s}$. There should be little feedthrough at HF. The inputs should be free from foldover, and the circuit unharmed by large overloads.

The main elements of the complete device are shown in Fig. 2. Note that all inputs, including the feedback to the op-amp summing point, are differential and have high impedance and low bias currents. This allows the device to be used, for example, as a two-quadrant divider with differential numerator and denominator. The high open-loop gain of the op amp ($\sim 20\,000$) is valuable in this application.

III. OVERALL DESIGN

Fig. 3 is a simplified schematic of the multiplier. The inputs V_x and V_y are converted to differential currents by the emitter-degenerated amplifiers. The products $I_x R_x$ and $I_y R_y$ are both equal to 13.3 V which results in the factors X and Y having peak excursions of ± 0.75 at the nominal full-scale input of $\pm 10\text{ V}$. These peak excursions are larger than usual (a common range for X is ± 0.4) and were used to achieve lower effective noise and offsets, and better drift performance. However, this calls for more careful design of the core (see Section IV) and results in greater nonlinearity in the input am-

² A discussion of multiplier accuracy specifications is found in *Nonlinear Circuits Handbook*, Analog Devices, Inc., P.O. Box 280, Norwood, Mass., 1974, pp. 209-211.

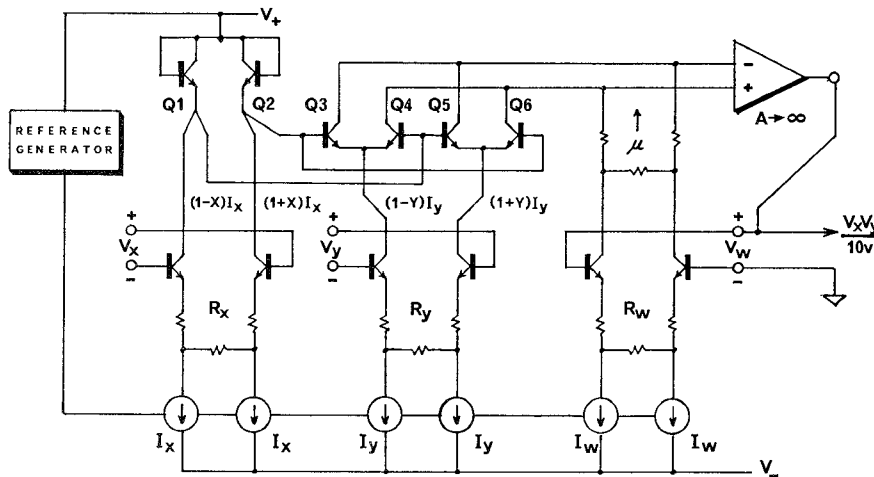


Fig. 3. Simplified schematic of the complete multiplier. Note the addition of an active feedback path.

plifiers. The latter can be substantially reduced by using a third amplifier to introduce the feedback round the op amp, having identical distortion characteristics to the X and Y stages. An analysis is given in Section VI.

The condition for loop balance is

$$\frac{V_x V_y}{I_x R_x R_y} = \mu \frac{V_w}{R_w} \quad (1)$$

where μ is the attenuation factor introduced by the π network in the collector circuit of the feedback stage, and is set equal to the peak-signal value of 0.75 for minimum distortion. $R_x = R_y = R_w = 88.5 \text{ k}\Omega$ total ($26 \text{ k}\Omega + 36.5 \text{ k}\Omega + 26 \text{ k}\Omega$), and $I_x = I_y = I_w = 150 \mu\text{A}$ nominal, controlled by the reference generator and trimmed to absorb resistor tolerances for a scaling voltage of exactly 10 V. Thus, in the multiplier connection the device conforms to the standard relationship $V_w = V_x V_y / 10 \text{ V}$. The connections for dividing, squaring, and square-rooting do not change the scaling voltage.

In addition to reducing the nonlinearities and providing a differential input to the summing-point, the active feedback scheme has the following advantages.

1) The insertion of an alpha in the feedback path provides full compensation for the alpha-error introduced by the Y-input amplifier.

2) The circuit has a very small offset sensitivity to the supply voltages, in the presence of resistor mismatch. By contrast, the usual "bridge" feedback, using resistors direct to the op-amp inputs (which are near V_+) has poor supply rejection unless the resistors are carefully matched.

3) The scaling-voltage can be easily changed (for example, to 1 V, giving a $\times 10$ gain compared to the usual connection) by inserting an external attenuator in the feedback path.

4) The normally grounded $-V_w$ connection can optionally be used to sum in an additional signal (up to $\pm 10 \text{ V}$) to the output.

Special care was taken to minimize errors due to variations of transistor current gain, which are par-

ticularly troublesome in the inverted form of the LTM core [Fig. 1(d)]. Details of the compensation method are contained in Section V.

The output op amp is conventional and will not be described here. It uses a lateral p-n-p input stage for level-shifting; no feedforward was used, resulting in a low unity-gain frequency point. However, the low transconductance of the first stage (which may be any one of the three emitter-degenerated amplifiers) allows a high slew rate to be achieved.

IV. ERRORS IN THE MULTIPLIER CORE

An analysis of the error sources has been previously given.³ The most important of these is undoubtedly V_{BE} matching, and this is dealt with at further length here, because it is the key to a successful implementation. The errors caused by a departure from the ideal case of isothermal nonresistive infinite-beta transistors are reviewed briefly.

V_{BE} (Emitter-Area) Mismatch

The large-signal linearity⁴ of multipliers based on two-quadrant elements such as Fig. 1(c) and (d) is critically dependent on V_{BE} matching. It is possible to devise transconductance multipliers in which this is not the case, or alternatively, to introduce linearity-correction adjustments. These approaches are usually more complex; some have inferior dynamics, or introduce additional noise or nonlinear terms; in some cases, they require more complex trimming procedures. Therefore the simple six-transistor core was retained, and several precautions taken to minimize mismatch.

It is convenient to assume that all V_{BE} errors are due

³ B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 365-373, Dec. 1968.

⁴ Strictly speaking, a multiplier is a nonlinear circuit, but the generally-accepted meaning of linearity in connection with multipliers is that measured when one input is held at a fixed value.

to differences in emitter area. Other sources, such as local variations in doping, dislocations, etc., can be converted into an equivalent area factor. This permits the definition of area-mismatch factors, which are easier to incorporate into analyses and have the advantage of being temperature-invariant. Thus, referring to Fig. 3, the emitter areas of Q_1 through Q_6 are designated A_1 through A_6 .

It is immediately apparent that there are two quite independent mismatch factors to consider. When V_y is very negative transistors Q_5 and Q_6 are inoperative, and consequently cannot contribute to the output. The area mismatch factor of the quad Q_1 - Q_2 - Q_3 - Q_4 is defined as

$$a_1 = \frac{1}{4} \left(1 - \frac{A_1 A_4}{A_2 A_3} \right). \quad (2)$$

This is a small number, usually within the range ± 0.005 . The equivalent V_{BE} error is given by

$$\Delta_1 V_{BE} = (V_{BE1} + V_{BE4} - V_{BE2} - V_{BE3}) \\ \approx \frac{4kT}{q} a_1, \quad \text{for } a_1 < 0.01. \quad (3)$$

Likewise, the quad Q_1 - Q_2 - Q_5 - Q_6 has an area mismatch factor

$$a_2 = \frac{1}{4} \left(1 - \frac{A_1 A_5}{A_2 A_6} \right) \quad (4)$$

and

$$\Delta_2 V_{BE} \approx \frac{4kT}{q} a_2. \quad (5)$$

Starting with the fundamental current-density equation shown in Fig. 1(b), the output of the core is found to be

$$Z = \frac{1}{X_{fs} Y_{fs}} [(X + a_1 + a_2)Y + (a_2 - a_1) \\ - \{Y(a_1 + a_2) + (a_1 - a_2)\}X^2] \quad (6)$$

where Z is the normalized output, full scale = ± 1 , X_{fs} is the chosen value for X at nominal FS input, and Y_{fs} is the chosen value for Y at nominal FS input. It is not essential for X_{fs} and Y_{fs} to be equal (they are often not) but in this design both are 0.75.

Equation (6) shows that in addition to the product term XY there is: 1) an X offset of $(a_1 + a_2)$; 2) an output offset of $(a_2 - a_1)$; 3) a parabolic error on the X input, which varies with the sign and magnitude of Y ; 4) no explicit Y offset; 5) no Y nonlinearity.

Closer inspection reveals that the magnitude of the parabolic error is proportional to the design value X_{fs} and the offsets and noise (the latter not included specifically) are inversely proportional to X_{fs} .

Eliminating the offsets in (6) by putting $Z_0 = (a_2 - a_1)$ and $X_0 = -(a_1 + a_2)$, we can examine the residual nonlinearity. The squared term becomes $(X + X_0)^2$, and this has the effect of inducing small Y -offset and scale errors, but these are also trimmable. The remaining error is

$$\epsilon(X, Y) = \frac{X^2}{X_{fs} Y_{fs}} [(a_2 - a_1) - Y(a_1 + a_2)]. \quad (7)$$

The " X feedthrough" of the fully trimmed device is simply the residual output when $Y = 0$ and X is varied from $-X_{fs}$ to $+X_{fs}$. Its peak value is therefore

$$\epsilon(X_{fs}, 0) = a_2 - a_1 \quad \text{relative to a FS output of } \pm 1. \quad (8)$$

Two points are of interest here. First, the X feedthrough can be zero, even though distortion is present for finite values of Y . Second, X feedthrough is not affected by the choice of X_{fs} and Y_{fs} .

When Y is at its FS value (± 0.75) the error is

$$\epsilon(X_{fs}, \pm Y_{fs}) = (a_2 - a_1) \mp 0.75 (a_1 + a_2). \quad (9)$$

The area mismatch factors can be of equal or opposite sign. In the first case, let $a_1 = a_2 = a$. Then the peak errors are $-1.5a$ for $+FS$ and $+1.5a$ for $-FS$ and the error is completely proportional to Y . In the second case, let $-a_1 = a_2 = a$. Then the error is a constant $2a$, independent of Y . This is clearly a worst case, and for ± 0.1 percent error, $a = 0.0005$, which in V_{BE} terms amounts to a mismatch of only $52 \mu V$ at $25^\circ C$.

It is worth stressing here that the existence of *two* independent mismatch factors prevents the use of a single adjustment to eliminate all nonlinearities. Some designs introduce a small voltage between the bases of Q_1 and Q_2 to eliminate X offset, but this trimming technique is dangerous, because it can actually introduce parabolic distortion when (as is often the case) all or some of this offset is caused by unbalances in the current-sources and X amplifier, requiring the core to be deliberately mismatched. Also, unless the correction voltage is proportional to temperature, the trim will introduce a drift term. Note that this technique also cannot change the parabolic feedthrough at $Y = 0$, and results in an X nonlinearity which is independent of the value of Y .

In the absence of adjustments, some means to ensure inherently low V_{BE} errors is sought. Quad layouts are sometimes used for this purpose.⁵ At first sight, though, this solution would appear to require a total of twelve transistors, raising formidable layout difficulties. But (2) and (4) show a way to avoid this. Note that linearity is preserved so long as $A_1 A_4 = A_2 A_3$ and $A_1 A_5 = A_2 A_6$. So it is not necessary for all the pairs to match. Indeed, it is demonstrably possible to obtain good linearity even when one device of each pair (e.g., Q_3 - Q_4) is twice that of the other. So, by arranging the transistors in two overlapping quads, sharing the inner pair Q_1 - Q_2 and cross-connecting to the bases of the outer pairs, quite large processing gradients can be tolerated. This "six-pack" layout for the core is clearly visible in the

⁵ M. A. Maidique, "A high-precision monolithic super-beta operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-7, pp. 480-487, Dec. 1972.

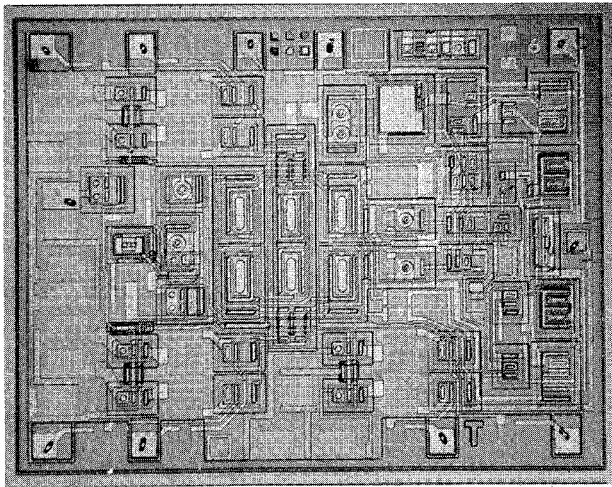


Fig. 4. Picture of the chip. The "six-pack" multiplier core is at the center, and the four output transistors of the op amp are on the far right.

picture of the chip, Fig. 4, which also shows the transistor geometry.

Optimum transistor design for this type of multiplier is almost totally a matter of preventing processing defects from disturbing the V_{BE} matching. As will be seen later, the devices do not need to have the very low ohmic resistances usually required of a logarithmic device. The large emitter areas used here are for the purpose of reducing the effects of fine-structure processing grain, such as poorly-etched edges; they have an area of $7100 \mu\text{m}^2$ and operate at a peak current-density of $4.2 \text{ A}\cdot\text{cm}^{-2}$, at which level the intrinsic transistor is near ideal. In preparing the $\times 500$ artwork, only one emitter outline was cut, then photorepeated six times and patched into the rubyliths.

A further possibility for improving V_{BE} matching is the use of a shallower emitter than usual, yielding betas with median values of about 200, rather than the 400–500 more typically achieved. This has the further advantage of improving the match of base resistance, and lowering the output conductance. The latter is a subtle source of parabolic nonlinearity in the input amplifiers, arising from variations of the current I_x as the input voltage varies through its full range of 20 V, when the multiplier is driven from a single-sided signal. Low-beta processing also increases the BV_{CEO} of those transistors operating at the full supply voltage, thus ensuring a good yield of devices to a high-voltage specification. The provision of full beta-compensation allows the use of low-beta processing without jeopardizing multiplier accuracy.

Thermal Gradients

The second most serious threat to accuracy is a difference of temperature between transistors in the core. Two types of errors can arise. The first is that due to a thermal gradient across the individual pairs Q_1 – Q_2 , Q_3 – Q_4 , Q_5 – Q_6 . This causes input offset errors of 400

$\text{mV}/^\circ\text{C}$ relative to the FS of $\pm 10 \text{ V}$. Put another way, only 0.025°C can be tolerated between a single pair to maintain an error of ± 0.1 percent of FS. The second kind of error is less serious. A gradient which causes the pairs Q_3 – Q_4 and Q_5 – Q_6 to be at a different net temperature to the pair Q_1 – Q_2 will introduce a cubic nonlinearity on the X input whose magnitude becomes ± 0.1 percent peak for a difference of less than 0.5°C . Thermal offsets do not cause Y nonlinearity.

The six pack minimizes the errors introduced by thermal gradients. If these are linear, offset errors for any vector direction exactly cancel (due to the cross connection). Linear gradients along the major axis introduce cubic errors into the two quads, but the low sensitivity prevents these being significant, and these cancel anyway near $Y = 0$. The low thermal sensitivity of the six pack is one of the improvements in chip design. Additionally, the core was located on what is effectively a thermal plateau at the center of the chip. The power dissipation of the surrounding circuits was arranged to be evenly distributed. The output transistors of the op amp were split into four separate devices and placed along the far edge of the chip, so that changes in load current have only a small effect on the thermal "wavefront."

Resistive Mismatch

It was shown in footnote 3 that it is not necessary for the transistors used in the core to have low resistances, as would be the case in many logarithmic circuits. It is interesting to note that this is an advantage of the "two-quadrant" forms, Fig. 1(c) and (d). By contrast, using the general forms of Fig. 1(a) and (b) in "one-quadrant" multiplier implementations (as in the "computing" rms converter, for example) small ohmic resistances introduce dramatic errors, whereas V_{BE} matching errors can be tolerated, as they affect only the scale factor.

While high ohmic resistances can be tolerated, these must match reasonably well, and since much of this resistance arises in the base circuit, this also implies that good beta-matching is required. Mismatch introduces cubic errors on the X input very similar in form to those caused by thermal gradients, in the case where the pairs Q_3 – Q_4 and/or Q_5 – Q_6 have a different ohmic resistance to the pair Q_1 – Q_2 . When the mismatch is between individual devices in the pairs, an input offset results. The latter is the more significant, for a 0.1 percent input error is caused by only 0.33Ω of mismatch. The large transistors used in the six pack have inherently low resistance, ensured by the long emitter geometry and wrap-around base contact. Low-beta processing further improves the match.

Metalization resistances are often a cause of error. Typically, the sheet resistance of the aluminum is $50 \text{ m}\Omega$ per square, and the interconnections must be carefully balanced. Note the way the emitters of Q_1 and Q_2

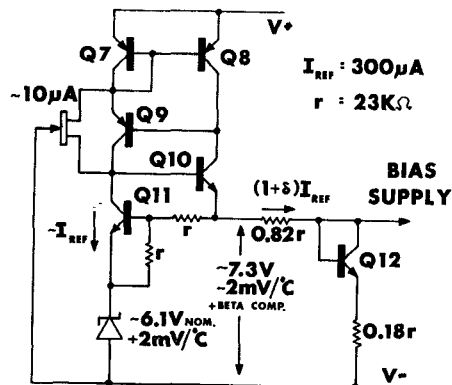


Fig. 5. Reference generator circuit. Q_{12} is part of the current-source circuits.

are connected, and the dummy lengths of metal inserted in the emitter leads of Q_3 - Q_4 and Q_5 - Q_6 .

Base Currents

Base currents in Q_3 through Q_6 are additive to the currents $(I + X)I_x$ and $(I - X)I_x$. This has the effect of increasing the scaling voltage, and the effect is not negligible. It is shown in the Appendix that the transfer function is multiplied by a factor $(1 - 3\delta)$, where $\delta = 1/\beta$. Assuming a worst-case beta of 100, this is a -3 percent scale error. This might be tolerable, but beta is not stable with temperature, and typically increases by 1 percent per $^{\circ}\text{C}$, thus causing a scale-factor drift of +0.03 percent per $^{\circ}\text{C}$ max. This is clearly not compatible with a 1 percent accuracy over a 180°C range. Fortunately, use can be made of the dependence of scale factor on I_x to introduce an identical $(1 - 3\delta)$ factor in the denominator of the transfer function, and thus achieve close compensation. This will be discussed in the next section.

V. SCALE-FACTOR STABILITY

The output of a two-signal multiplier having voltage inputs must be scaled by a denominator having the dimension of voltage. A self-contained unit must therefore include a voltage-reference element of adequate stability. Reverse-biased emitter-base junctions are often used, but these generate significant amounts of noise unless driven at high current densities, which appear as modulation noise at the output. They also are subject to long-term drift. This design uses the breakdown between the emitter diffusion and the base-enriched isolation diffusion, resulting in a planar bulk junction. The voltage is referenced to the substrate, resulting in a very simple structure. The breakdown voltage is nominally 6.1 V and the temperature coefficient (TC) approximately +2 mV/ $^{\circ}\text{C}$.

Fig. 5 shows the complete reference generator, which includes compensation for the TC's of the reference diode and the diode Q_{12} which forms part of the current sources for the multiplier. The resistors in the base circuit of Q_{11} multiply its V_{BE} . They are thin-film re-

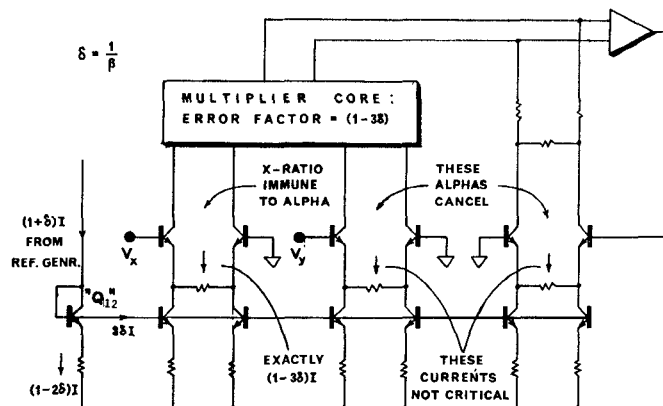


Fig. 6. Details of the beta-compensation technique.

sistors, and may be adjusted for exact temperature compensation by changes to the metalization; as shown, they are correct for a breakdown TC of +2 mV/ $^{\circ}\text{C}$, but the range of adjustment can absorb any TC from zero to about +5 mV/ $^{\circ}\text{C}$. The bias current I_{REF} is supplied by Q_{10} and the collector current of this transistor is inverted by the Wilson current-mirror Q_7 - Q_8 - Q_9 . Consequently, the bias current for the reference diode is self-stabilizing, resulting in a well-defined, supply-insensitive operating point. A small epi-FET is included to ensure start-up; its channel current is uncritical, and may range from a few nanoamps to about 100 μA . The finite channel conductance has very little effect on supply rejection, due to its location across Q_9 , which has the effect of multiplying the slope resistance of the FET by the p-n-p beta. Typical devices show a variation of only 0.4 mV in the voltage at the emitter of Q_{12} for a supply voltage variation of 20 V. This corresponds to a scale factor variation of less than ± 0.02 percent over the supply-voltage range ± 10 to ± 20 V.

Beta Compensation

Exact compensation for the errors caused by finite current-gain in all the signal-path transistors requires a careful assessment of their interactions. Fig. 6 shows the overall scheme in a way that highlights these errors. First note that bias currents in the Y and W amplifiers do not have any direct effect on scale factor; they are made equal to the X-amplifier bias current in order to minimize cubic distortion terms. Second, the alpha errors in the forward path through the Y amplifier are cancelled by those in the feedback path through the W amplifier. Third, it is important to realize that the alphas of the X amplifier transistors do not appear as scale-factor errors. This is because the X input of the multiplier core is *ratio dependent*, and the ratio is determined in the *emitter* circuit of the X amplifier and preserved exactly in the collector circuit even when alpha is low. A severe alpha mismatch can introduce parabolic distortion on this input, but the magnitude is small; a 10 percent mismatch in a beta of 100 causes less than 0.1 percent distortion.

These considerations show that only the basic $(1 - 3\delta)$ error of the core remains. If the bias current to the X amplifier is multiplied by the same factor, compensation is achieved. Now, the six current sources supply a total of $900 \mu\text{A}$, and the bias current to Q_{12} is nominally $300 \mu\text{A}$. Consideration of the current terms shows this amounts to an error of $(1 - 4\delta)$. To avoid raising the input bias to $450 \mu\text{A}$ and get the right factor this way, an additional compensation term is added to the input bias current. This is the reason for choosing the value of resistor in the base of Q_{11} to be equal to the sum of the bias resistors, because the base current of Q_{11} is δI_{REF} , and this raises the bias current to $(1 + \delta)I_{\text{REF}}$. For the compensation to be perfect, Q_{11} ought really to operate at exactly the same current-density as the transistors in the multiplier core; as a compromise, the emitter area of this transistor was raised to $2600 \mu\text{m}^2$. Note that the reference diode actually operates at $I_{\text{REF}} + V_{\text{BE}}/r$, which is not temperature-stable. However, the TC of the breakdown voltage is not critically dependent on the current density, and a slight shift in the TC due to this effect is absorbed by the initial TC adjustment.

VI. INPUT-AMPLIFIER DISTORTION

Simple emitter-degenerated voltage-to-current converters introduce odd-order distortion, due to the current-dependence of the two V_{BE} 's. Incidentally, this so-called "S-shaped" distortion is often incorrectly blamed on the transconductance core and described as "typical Y -input distortion." The fact is, it occurs on both X and Y inputs, but in the former case it is usually masked by other nonlinearities, or is less because of the smaller current swings used in the X amplifier.

While it is not possible to give a closed-form solution for the input-stage distortion, it is easy to relate the input voltage required to set up a particular current ratio, and analyze the distortion with this as the dependent variable. Referring to Fig. 7, which is a simplified form of the multiplier in which the core has been replaced by a variable attenuator, we can write the inputs as

$$V_y = YIR + \frac{kT}{q} \ln \frac{1+Y}{1-Y} \quad (10)$$

and

$$V_w = WIR + \frac{kT}{q} \ln \frac{1+W}{1+W}. \quad (11)$$

In each case, the first term represents the linear relationship and the second term is the nonlinear voltage introduced by the difference of V_{BE} . Not all of this second term is nonlinear, however, for it includes the small signal r_e (the value when $Y = W = 0$), which is $2kT/qI$ in series with the large resistors R . Rewriting (10), we can separate the linear and nonlinear terms as

$$V_y = YI\left(R + \frac{2kT}{qI}\right) + \frac{kT}{q} \left(\ln \frac{1+Y}{1-Y} - 2Y\right) \quad (12)$$

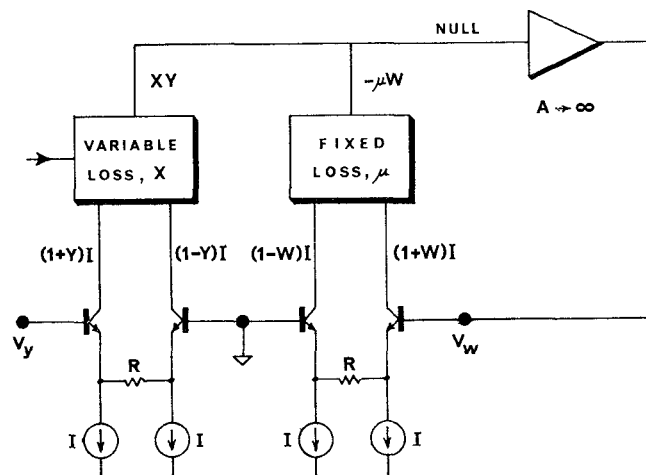


Fig. 7. Basic active feedback scheme. The "variable loss" element is the multiplier core, and the variable X corresponds to that input of the multiplier.

and a corresponding expression can be written for V_w . Inserting the peak values used for Y and W (± 0.75), the nonlinear component is found to be $\pm 11.6 \text{ mV}$ at 25°C , or about 0.12 percent of FS.

It is intuitively obvious that if the fixed loss μ and the variable loss X are equal, the nonlinearities will exactly cancel. This has been experimentally confirmed, and nonlinearities of less than 0.001 percent of FS measured, using purely resistive elements to introduce the variable loss (or with both attenuators removed). This suggests the possibility of making a very precise unity-gain amplifier with differential input and output, having independent common-mode levels.

We must now determine how effective the cancellation is when X and μ are not equal, by deriving expressions for the distortion between the Y input and the W input with X as a parameter. The system is completely symmetrical in this respect, however, and the distortion from the X input with Y as a parameter merely requires a change of labels.

The input to the op amp is nulled when $W = XY/\mu$, so this value of W can be substituted in the equation for V_w to find the actual output voltage. The exact output voltage in the absence of distortion would be XV_y/μ . The error voltage is therefore

$$\epsilon(X, Y) = (\text{actual value of } V_w) - (\text{exact value of } V_w)$$

and making the substitution $X/\mu = K$ (where $K = 1$ at FS), and inserting these variables into (10) and (11), the linear terms cancel to leave

$$\epsilon(K, Y) = \frac{kT}{q} \ln \left(\frac{1+KY}{1-KY} \right) \left(\frac{1-Y}{1+Y} \right)^K. \quad (13)$$

This expression gives the absolute error as a function of the internal variable Y (which is very nearly linear with respect to V_y). By equating the derivative of $\epsilon(K, Y)$ to zero, the value of K at which the error is greatest is found to be

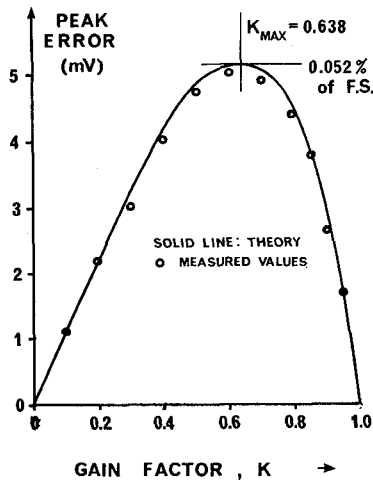


Fig. 8. Theoretical and measured peak error of the active feedback scheme.

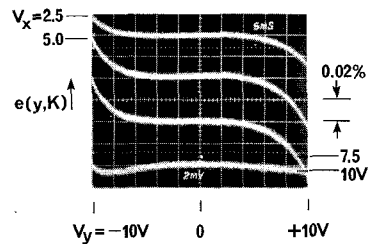


Fig. 9. Residual Y nonlinearity for four values of X_x . Multiple-exposures with vertical shift between exposures. Approximately 0.007 percent parabolic distortion is visible at $V_x = 10$ V, possibly due to a small beta mismatch.

$$K = \left(\frac{1}{Y^2} - \frac{1}{Y \tanh^{-1} Y} \right)^{1/2} \quad (14)$$

Using the FS value of 0.75 for Y yields $K = 0.638$, that is, $V_x = \pm 6.38$ V. With this value for K put back into (13) the maximum absolute error is found to be -5.18 mV; in other words, the output is never more than 0.052 percent of FS below the theoretical value. The nonlinearity is actually about half this because some of the error can be absorbed by a gain trim.

Fig. 8 shows the peak absolute error at $V_y = \pm 10$ V as a function of K . These results were obtained using a prototype monolithic device; the form of the error is shown in Fig. 9, for four values of V_x . Of course, when $V_x = 0$ there is no residual error. Note that the residual error at $V_x = 10$ V, amounting to about ± 0.005 percent, is the *total* error for the complete device including the multiplier core and op amp. This validates the claim that there is inherently no distortion in the Y channel of the intrinsic transconductance multiplier.

VII. PERFORMANCE

The performance of early prototype chips verifies the effectiveness of the error-reducing design. Most notable is the "theoretical" appearance of the residual

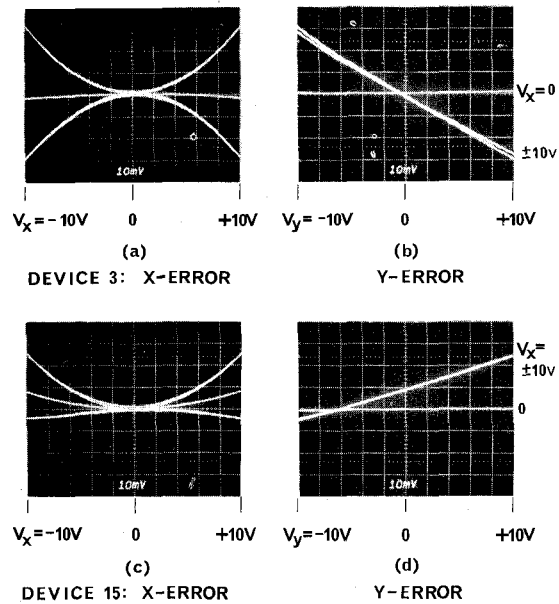


Fig. 10. Error cross-plots for two fully-trimmed units. Multiple-exposures with no shift between exposures. Device 3 has area-mismatch factors which are closely equal in sign and magnitude, hence cancel for $V_y = 0$. Device 15 shows one mismatch factor which is nearly zero (at $V_y = -10$ V).

errors when displayed on an oscilloscope. With the X input set to FS (± 10 V) the Y nonlinearity is within ± 0.01 percent for most samples; with the Y input set to ± 10 V, the only visible errors are the residual parabolic terms. The available data indicate that the six pack layout is yielding better matching, some devices meeting the full test standards for a 0.1 percent multiplier. Further statistical data are needed to properly appraise this. Fig. 10 shows some representative cross plots; notice that the residual linear errors in Fig. 10(b) and (d) are the result of the parabolic X error, and conform to the predictions of (7).

The temperature dependence of scale factor has been measured; the results are shown in Fig. 11. The downward curvature at high temperature is believed to be due to a parasitic MOS effect, which has since been rectified. The untrimmed scaling-voltage spreads from approximately 9.5 to 11 V, and the measured TC over the range 0 to $+70^\circ\text{C}$ is fairly independent of the voltage, being about $+75 \pm 25$ ppm/ $^\circ\text{C}$ with the initial compensation ratios.

The measured noise referred to the output is approximately $400 \mu\text{V}$ (rms) over 20 Hz to 250 kHz, and was found to be substantially independent of signal level. This suggests that the reference supply is noise free, and this was confirmed by measuring the open-circuit voltage at pin 4, where the reference voltage is about 1.2 V and the noise level is below $10 \mu\text{V}$ (rms).

Considerable improvement in the feedthrough of signals at HF is seen. Fig. 12 shows the swept-frequency response with one input being nulled and the other a 20 V (peak to peak) sine wave from about 10 to 500 kHz. The HF feedthrough is usually lower on the X input

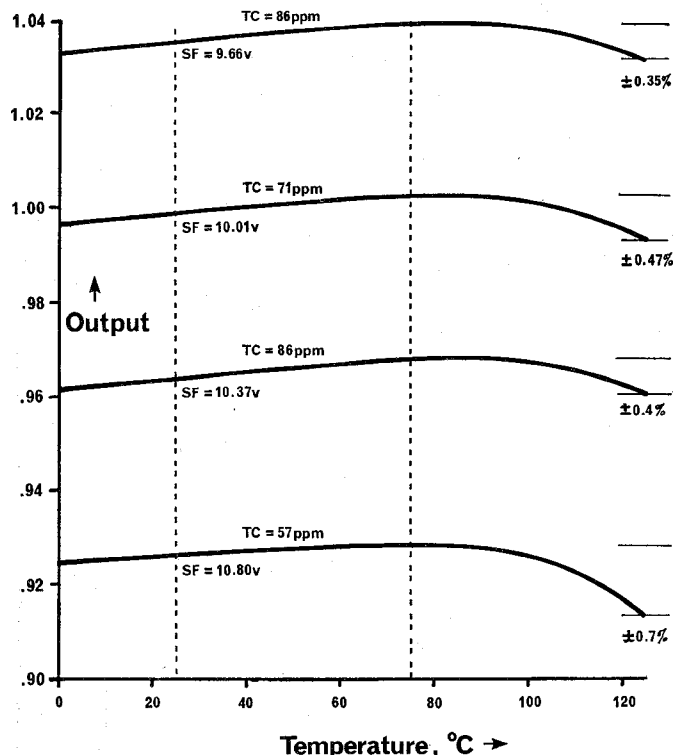


Fig. 11. Variation of scale-factor with temperature. Conditions were $V_x = +10$ V, $V_y = 1$ V (rms), $V_s = \pm 15$ V. No trimming was applied, so some error may be due to drift of the X input.

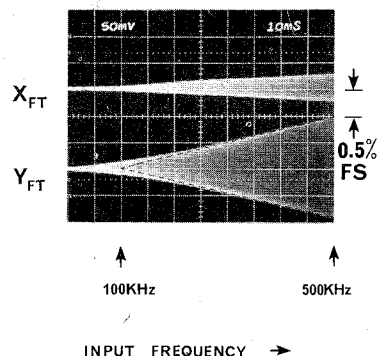


Fig. 12. Typical HF feedthrough; for one input nulled, the driven with 20 V (peak to peak).

of a transconductance multiplier, as is the case here. This is due to the cancellation of currents in the collector-base capacitances of the transistors Q_3 through Q_6 in the multiplier core.

Table I lists other key performance parameters.

VIII. CONCLUSION

It has been demonstrated that the linear transconductance multiplier is capable of accuracy specifications considerably higher than generally accepted, and the gap between this technique and the most important alternative high-accuracy technique of pulse-width-height modulation is narrowing. The wider bandwidth of the LTM, the absence of need for any external com-

TABLE I

PERFORMANCE (MULTIPLIER CONNECTION, $V_s = \pm 15$ V, 25°C)

Overall accuracy	± 0.25 percent of FS
Scale-factor temperature coefficient	$+75$ ppm/ $^\circ\text{C}$
Scale-factor supply sensitivity	< 0.002 percent/V
Output noise (signal-insensitive)	
20 Hz–250 kHz bandwidth	400 $\mu\text{V(rms)}$
Small-signal bandwidth	1.2 MHz
Slew rate	30 V/ μs
X nonlinearity	
($Y = +10$ V, $X = -10$ to $+10$ V)	0.15 percent of FS
Y nonlinearity	
($X = +10$ V, $Y = -10$ to $+10$ V)	< 0.01 percent of FS
Input offset current	
(all input pairs)	40 nA
Input offset voltage drift	< 100 $\mu\text{V}/^\circ\text{C}$

ponents, and the freedom from residual carrier components on the output will continue to be its main advantage. Future improvements in precision bipolar technology will almost certainly result in accuracies of 0.1 percent becoming commonplace.

When used as variable-gain elements, four-quadrant multipliers are typically limited to a control range of $20:1$, because of the detrimental effect of drift. This design has reduced drift by a factor of approximately five, providing an extension of the control range to at least $100:1$, and reduced feedthrough to about -60 dBs at 100 kHz. However, specially designed two-quadrant multiplier/divider units are better suited to variable-gain applications.

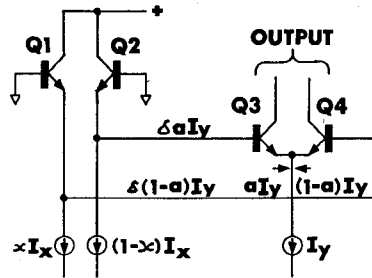


Fig. 13. Basic core for analysis of beta errors.

The one remaining fundamental drawback of the LTM technique is the intrinsically high noise level of the basic circuit. By using much more of the available dynamic range this design has achieved a reduction by a factor of about 3, to a level of -85 dBs referred to FS output. For applications where noise is critical, multipliers based on carrier-domain principles are promising.⁶

APPENDIX

BETA ERRORS IN CORE

Fig. 13 shows a "half-multiplier" for analysis; the results are easily extensible to the full circuit. The fundamental relationship is

$$J_1 J_2 = J_3 J_4. \quad (A1)$$

Assuming equal emitter areas, and noting that the emitter currents of Q_1 and Q_4 are increased by the base currents of Q_2 and Q_3 , we can write

$$\begin{aligned} [xI_x + \delta(1-a)I_y][(1-a)I_y] \\ = [aI_y][(1-x)I_x + \delta aI_y] \end{aligned} \quad (A2)$$

where δ is the base-defect term, I_B/I_E .

⁶ B. Gilbert, "New planar distributed devices based on a domain principle," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 1971, p. 166.

This yields

$$a = \frac{x + \delta}{1 + 2\delta}. \quad (A3)$$

For $x = 0.5$ (input balanced), $a = 0.5$ (output is balanced) for any δ ; that is, base currents do not cause offsets, unless the base-defect terms are substantially different. So, $da/dx = (1 + 2\delta)^{-1}$, or (since $\delta \ll 1$), $(1 - 2\delta)$.

Since the output is from the collectors of Q_2 and Q_3 , an additional $(1 - \delta)$ term is introduced, yielding an overall gain error of $(1 - 2\delta)(1 - \delta) \approx (1 - 3\delta)$.

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