

A Versatile Monolithic Voltage-to-Frequency Converter

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Abstract—Voltage-to-frequency (V - F) conversion is achieved with high linearity (0.02 percent) using a precise multivibrator with an 80-dB dynamic range. The IC operates from a single, low-current supply and can accept millivolt signals. A unique thermometer output permits direct conversion of temperature to frequency.

I. INTRODUCTION

A MONOLITHIC circuit has been developed which provides accurate voltage-to-frequency (V - F) conversion at low cost and with the minimum number of external parts: a timing capacitor and a scaling resistor. Any full-scale (FS) frequency up to 200 kHz and FS input from 100 mV to over 30 V can be chosen, with a simple scaling relationship. Good linearity has been achieved using a new multivibrator design which, in conjunction with a bandgap reference circuit, is temperature-compensated to ± 30 ppm/ $^{\circ}\text{C}$. The multivibrator uses adaptive biasing to operate over a 20 000:1 frequency range with a given timing capacitor, and generates a square-wave output. This is often more useful than the narrow pulse generated by charge-dispersing V - F converters; for example, it allows the circuit to be used as the voltage-controlled oscillator (VCO) in precision phase-locked loops. It also ensures constant chip dissipation with variation in frequency, important when driving the maximum load current of 30 mA at the maximum supply of 36 V. Single-supply operation down to 4.5 V at a quiescent current of only 1.2 mA are valuable assets in battery-powered equipment. The high sensitivity and low drift of the input amplifier permit direct interfacing with low-level transducers such as thermocouples and strain gauges, while the high input impedance (250 M Ω typical) accommodates such signals as generated by potentiometric transducers. Either positive or negative inputs can be accepted; dual supplies allow operation from differential signals above or below ground level.

A unique feature is the provision of an output voltage scaled $+1$ mV/K. The IC can thus operate as a thermometer delivering a frequency directly proportional to absolute temperature. The low dissipation is an essential prerequisite in this mode. A fixed reference-voltage output of 1.00 V is also provided, having a variety of uses. For example, in the thermometer mode it can be used to offset the scale to read directly in degrees Fahrenheit or centigrade with a typical scaling factor of 10 Hz/degree. It may also be used to power resistive transducers, set up other scale offsets (for example, in converting a 4–20 mA input signal to a 0–10 kHz output), or define a stable fixed frequency. A controlled temperature coefficient (TC) of

up to ± 250 ppm/ $^{\circ}\text{C}$ or more can be introduced to compensate for some external temperature sensitivity, using these outputs in combination.

Very few external components are required to realize all of the major operating modes. However, by adding a quad op amp, very exact ratiometric operation can be achieved (± 0.1 percent accuracy in the division of two analog inputs over a 10:1 denominator range and 10 000:1 numerator range). A precision phase-locked loop requires the addition of just a quad NAND gate, providing ultralinear frequency-to-voltage conversion (Section VIII).

Fig. 1 shows the main sections of the V - F converter in block-diagram form.

II. BACKGROUND

A V - F converter must exhibit high linearity (<0.1 percent of FS deviation from zero-based straight line) over a dynamic range of at least 10 000:1, with good temperature stability (<100 ppm frequency drift per degree centigrade) and supply-rejection (<100 ppm per volt). Since the introduction of the precision charge-dispersing technique [1], which can meet these requirements with ease, alternative approaches based on classical relaxation oscillator techniques have been somewhat in eclipse. Nevertheless, one of these, the symmetrical emitter-timed astable multivibrator, has attractive features. It is simple, needing only a single capacitor for timing, and ideally suited to monolithic fabrication; its push-pull configuration results in large charging voltages being available across the capacitor even at low supply voltages for improved stability and jitter; its square-wave output is generally more useful than the pulse output of a charge-dispersing converter; the tight coupling within the regenerative loop minimizes nonlinearity caused by transit-time and switching delays.

Prevalent designs have tended to cast doubt on the applicability of multivibrators to V - F conversion, and their use has been most successful as the current-controlled oscillator in monolithic phase-locked loops. The earliest IC's had poor temperature stability and totally inadequate dynamic range and linearity for V - F applications [2]. With improved attention to the mechanisms which define these characteristics a dynamic range of about 1000:1 and a stability of ± 20 ppm/ $^{\circ}\text{C}$ was achieved by the author in a second-generation PLL circuit [3]. Concurrently (1971) the design of a 15 MHz emitter-timed circuit using precision collector clamping was in progress, and the design presented in this paper is an extension of that work. Recently, a design bearing some similarity has been published by Cordell and Garrett [4], and a brief comparison is merited. In their circuit, the junction voltages developed across the collector-catching diodes are used to define the capacitor charging voltage directly (that is, no precise reference voltage is supplied in the collector circuit) which consequently

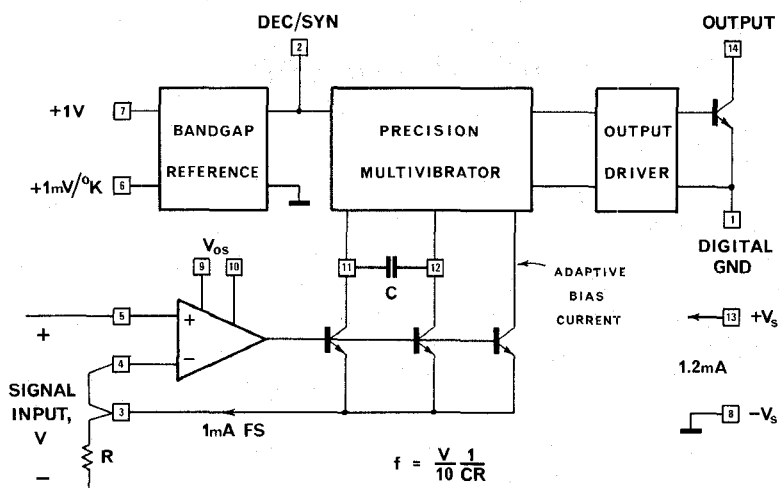
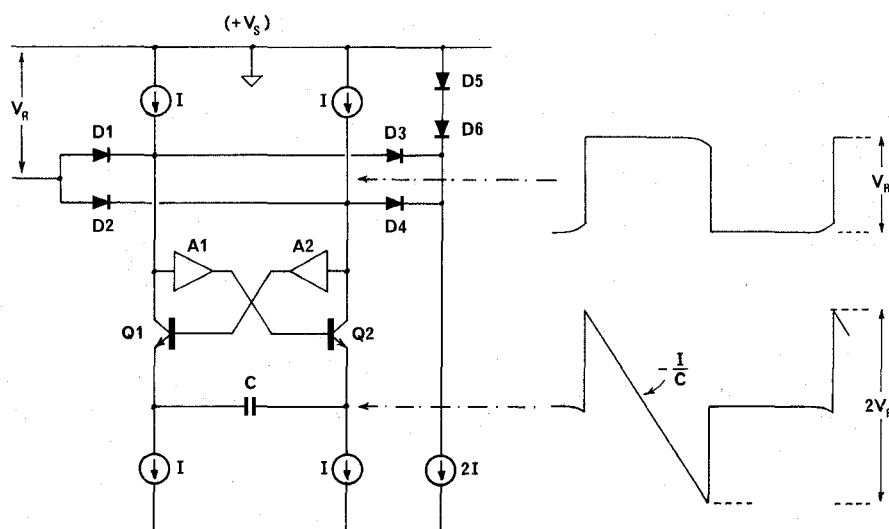
Fig. 1. Block diagram of the V - F converter.

Fig. 2. The basic multivibrator showing precision collector clamping.

has a very large temperature dependence (about -3000 ppm/ $^{\circ}\text{C}$). A special current generator, having the same nominal TC, is then used to charge the capacitor. The compensation is exact only at the center frequency, determined by an external resistor, since the control current which modulates the frequency is not compensated, and even quite small deviations degrade the TC (typically ± 300 ppm/ $^{\circ}\text{C}$ at a ± 10 percent deviation). The technique is suitable for some PLL applications, where the resulting temperature dependence of the control characteristic can be tolerated, but in order to use the circuit in V - F conversion it would be necessary to interpose a one-quadrant current-mode multiplier in the control-current path, to scale the timing current by a junction voltage. The approach adopted in the circuit to be described ensures that the collector clamping potentials are exact, and controlled by a known reference voltage. The capacitor

charging current is provided by a very linear voltage-to-current interface. The only temperature compensation required is to eliminate a small (230 ppm/ $^{\circ}\text{C}$) drift of fundamental origin. This is a point of detail which seems to have been overlooked in previously published work on the emitter-timed species, although the exact magnitude of the drift depends on the particular configuration.

III. PRECISION COLLECTOR-CLAMPED MULTIVIBRATOR

The basic wide-range oscillator is shown in Fig. 2. A1 and A2 are two-stage emitter-followers which provide high current-gain (hence, loadable output nodes) and level-shifting. The input transistors are biased with currents which track the timing current, resulting in a small, ratiometric loading of the collector nodes. The collector-clamping arrangement transfers a precise reference voltage V_R to the timing capacitor via Q1

and $Q2$. This voltage is normally provided by the bandgap circuit, but can alternatively be supplied from an external source, allowing the linear control of period.

The operation can be followed with the aid of the waveforms in Fig. 2. (The $+V_s$ supply is shown grounded for simplicity.) Assume $Q1$ is conducting. Its emitter current is $2I$, and the charging current I flows from left to right in the capacitor. $D1$ is conducting, clamping the collector of $Q1$ at $-(V_R + \phi)$, where ϕ is the base-emitter voltage of this diode-connected transistor at the current I . $Q2$ is nonconducting, so its collector is clamped by $D4$, and since the identical diodes $D5$ and $D6$ all conduct the current I , the collector of $Q2$ is at $-\phi$. Thus, a differential voltage of exactly V_R appears across the collectors, independent of the current, the temperature, the absolute value of ϕ , or the supply voltage. This ideal is impaired by junction offset-voltages, inaccuracies in the secondary current-sources, and loading by $A1$ and $A2$. However, the effects are minimal; for example, a composite error of 3 percent in the current-ratio factor that includes all of the forward-biased junctions causes an absolute error of about 0.1 percent in V_R and a TC-offset of 3 ppm/ $^{\circ}\text{C}$, a figure readily attained by the full design. Errors in the collector clamping potentials are practically independent of current, and do not jeopardize linearity.

In the emitter circuit the capacitor charges until $Q2$ begins to conduct. At a critical point regenerative switching occurs and the polarity of the differential collector voltage and the timing current reverse, beginning the next half-cycle. Neglecting second-order effects the capacitor charges through $2V_R$ twice each cycle, so the frequency of oscillation is

$$f = \frac{I}{4CV_R} \quad (1)$$

The current I is actually one third of the control current, that is, $I = V/3R$, where V is the control voltage and R is the external scaling resistor. With $V_R = 833$ mV, the overall control relationship becomes

$$f = \frac{V/3R}{4C \times 0.833} = \frac{V}{10CR} \quad (2)$$

For the common case of a 10 V FS input, the FS frequency is simply $1/CR$. The design is optimized for a control current of 1 mA FS, that is, a timing current range of 33 nA to 333 μA for an 80 dB dynamic range.

A. Dynamic Range

The "current-mode" nature of the collector-clamping system, and the high current-gain of the buffer stages $A1$ and $A2$, result in a dynamic range which is limited more by the quality of processing (affecting such parameters as low-current beta and surface leakage paths) and the allowable nonlinearity, than by the configuration. At very low values of timing current combined with high temperatures, the junction saturation currents cause frequency errors and, ultimately, cessation of oscillation. This is not expected to be a problem of much practical concern, and very similar effects limit the dynamic

range of charge-dispensing converters (for example, the input bias-current and offset voltage at the current-summing input node). Measurements on the monolithic parts have shown that the period can be as long as 20 s on the 10-kHz range, corresponding to a timing current of only 1.5 nA (control-current input of 4.5 nA).

The upper limit of the dynamic range is determined mainly by power dissipation constraints, if linearity errors are of no consequence. In the complete design, the control current is deliberately limited to 5 mA. This suggests that a dynamic range of over one million is possible. However, in V - F applications a maximum input of 1.5 mA is recommended, and the circuit is not specified for an input of less than 100 nA, a guaranteed dynamic range of 15 000:1.

B. Temperature Coefficient

The simplified analysis took no account of the logarithmic junction characteristics and assumed abrupt switching after a capacitor rundown of $2V_R$, which would be true only at absolute zero temperature. The regenerative process under less frigid conditions is quite complex, and Appendix I shows that switching occurs after a transitional phase during which the charging current falls to $(\sqrt{3} - 1)I$. This causes the junction currents to be unequal at the switching instant, and the voltage swing across the capacitor is less than $2V_R$ by an amount proportional to absolute temperature (PTAT), due to the kT/q term in the junction offset voltages. While this shortens the period, the falloff in charging current during the transitional phase lengthens it. Overall, there is a net reduction in period with increasing temperature by an amount which is theoretically 230 ppm/K and in practice has been measured as 270 to 330 ppm/K. The compensation technique consists of adding a small PTAT component to the temperature-stable V_R , both of which are generated by the bandgap circuit which tracks the oscillator temperature. Initially, the compensation voltage was set at 84 mV at 300 K. Although there is some disparity in the measured and theoretical drifts, it is significant that a single PTAT correction can result in very low residual drift with only slight curvature.

C. Linearity

The linearity of a V - F converter is specified as a percentage of the FS frequency, so that the effect of absolute errors becomes progressively less down-scale. It has been found that the most troublesome operating region is from about midscale upward, where the logarithmic conformance of the junctions is less exact. The peak capacitor swing is only 1.666 V, and a 500- μV error therefore amounts to a nonlinearity of 0.03 percent. Thus, very low excess ohmic resistance can be tolerated, particularly in $Q1$ and $Q2$, which are six-emitter transistors. Excess voltage in the diode-connected transistors $D1$ through $D6$ does not affect the transfer of V_R into the collector circuit because their forward voltages cancel, but their resistance will have a small effect on the switching point by raising the loop gain and thus causing regeneration to occur slightly earlier.

In practice, resistance in series with the capacitor is of more serious concern. It can be shown that

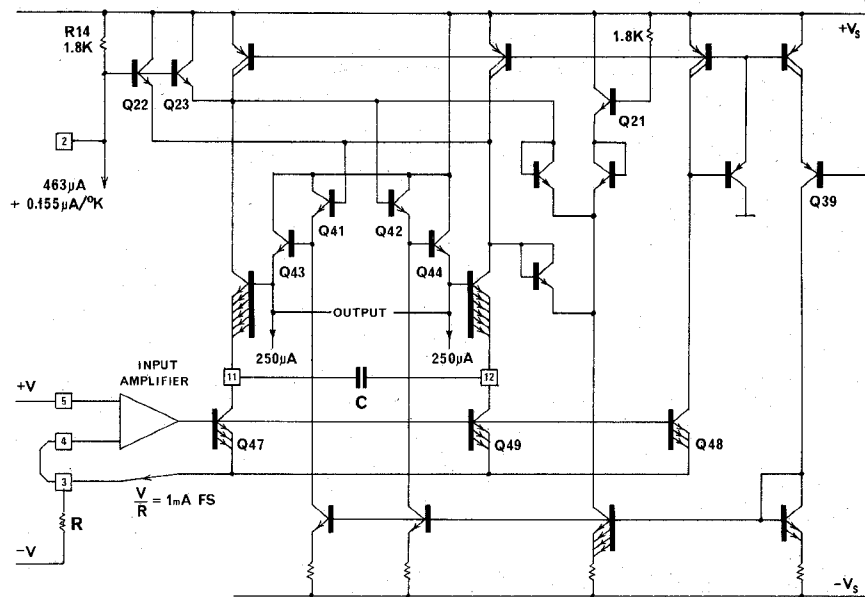


Fig. 3. Main components of complete precision multivibrator.

$$f' = \frac{1}{CR} \left(\alpha + \frac{2r}{R} \alpha^2 \right) \quad (3)$$

where $\alpha = V/10$ and r is the total resistance in the capacitor leads. Thus, for $r = 1 \Omega$ and $R = 10 \text{ k}\Omega$, the frequency would be 0.02 percent high at FS. Normally, the converter would be trimmed for exact frequency at FS, and there would be a residual parabolic error, having a peak value of $-50 \text{ ppm}/\Omega$ at midscale.

D. Complete Circuit

Fig. 3 shows the complete multivibrator and the interface with the voltage-to-current converter. The peak negative voltage at the capacitor nodes is typically 3.5 V below the $+V_s$ supply, so the timing currents can be coupled directly from the output transistors of the input interface (Q47 and Q49) avoiding the extensive use of current-mirrors with their attendant scaling errors, nonlinearity, and supply sensitivity. The less crucial secondary currents are derived with current mirrors, using the collector current of Q48 as the primary supply. The input interface is discussed in the next section.

The clamping diodes D1 and D2 (Fig. 2) become Q22 and Q23, whose current gain is utilized; the temperature-corrected reference voltage is generated by a composite current from the bandgap generator and converted to a voltage across R14 (1.8 k Ω), providing a node (pin 2) which can be driven by an external current or voltage to alter the scaling. Base current errors are minimized by an equal resistor in the base of Q21 (=D5 of Fig. 2). Beta mismatch in these transistors causes a parabolic nonlinearity: a 10 percent mismatch in a nominal beta of 400 introduces a peak error of ± 0.005 percent at midscale. Note that the reference-voltage input is differential (between the bases of Q22/23 and Q21), and a preferable compensation method would be to apply the (opposite-polarity) compensation voltage to Q21. This would have the

advantage that the control of period on pin 2 would be linear through zero, and the control voltage would require no compensation.

IV. INPUT INTERFACE

A current-controlled oscillator, however linear, is of no use as a voltage-to-frequency converter. An input interface is needed for voltage-to-current conversion, the performance requirements of which include the following.

- 1) Operation in either a high-impedance ("voltage-follower") or low-impedance ("current-summing") mode.
- 2) An input range which extends down to the $-V_s$ supply.
- 3) Good common-mode rejection to ensure linearity in the high-impedance mode.
- 4) Sufficient open-loop gain to ensure linearity at high scale sensitivities.
- 5) Low drift, commensurate with millivolt sensitivities.
- 6) Short-circuit protection of the current-summing node.

In addition, the interface circuit should have small bias currents, a current transfer ratio very close to unity, and be internally stabilized for ease of use. Response speed can be relatively low.

Fig. 4 shows the main details of the interface amplifier. In most applications the current input node (pin 3) and the voltage sense node (pin 4) are strapped and the scaling resistor is returned to ground. When the device is used at high sensitivities, separate force and sense connections can be used to eliminate lead-resistance effects. Ideally, the output transistors, Q47-49, would be Darlington connected (with the intermediate bases strapped to maintain good accuracy of current division) to minimize the effect of beta modulation as V_{ce} varies when the device is used in the high-impedance mode. However, there is only 400 mV of V_{ce} available when using a 5-V supply and the input is at +1.1 V, which not only prevents the use of Darlington's but also leaves no room for current-

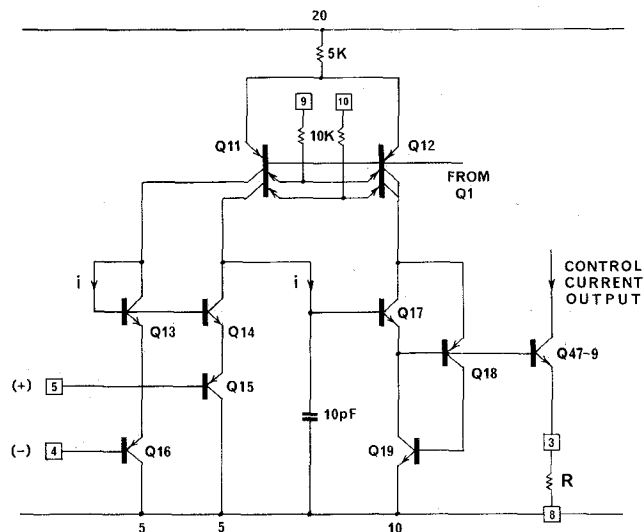


Fig. 4. The input interface (voltage to current converter).

limiting using an emitter sense resistor. Single transistors are therefore used, with controlled base-current drive to limit the short-circuit current to a value between 2.5 and 10 mA, this being a tight enough control for the application which must guarantee an input-current capacity to 1.5 mA and sensibly limit dissipation in the event of the current-summing input being grounded while pin 5 is elevated. The alpha error of the trio is compensated by the equal error of Q9 in the reference generator (Fig. 7); all of these transistors experience the same variation of collector voltage with supply variations. Emitter-area mismatch in Q47-49 can have several effects, depending on how the mismatches are distributed, including a scaling error, waveform asymmetry, and a small temperature drift (due to imperfect balance in the clamping currents). None of these effects has been troublesome, but to reduce the possibility of errors the transistors are multiemitter devices and operate at the same mean V_{ce} .

A. Gain Requirement

Nonlinear variation in the V_{be} of the trio is reduced by the open-loop gain of the amplifier, but it is not intuitively obvious how large this gain must be to achieve a given peak nonlinearity after scale and zero adjustments. This is analyzed in Appendix II; the main result of which is this expression for the peak error

$$\hat{e}_n = \frac{kT}{qG_o} \left[\ln \frac{\sigma}{\ln \sigma} - 1 \right] \quad (4)$$

where σ is the ratio of FS frequency to the frequency at which the "zero" adjustment is made, and G_o is the open-loop gain. A typical example is given in Fig. 5 for the case where the circuit is trimmed at FS and one-thousandth FS (that is, $\sigma = 1000$). The peak open-loop error is 103 mV at 300 K, and to reduce this to 0.01 percent of a FS input of 1 V requires $G_o = 1000$. To take another example, assume an FS input of 100 mV and a zero adjustment made at 1 mV. The peak

open-loop error is then 54 mV, requiring a gain of 5400 to be reduced to 10 μ V, again 0.01 percent of FS.

B. Input Stage

Vertical p-n-p transistors (Q15 and Q16) provide an input range down to $-V_s$ and also contribute to the low-drift performance when operating with appreciable source resistance. The beta of these transistors is only slightly temperature dependent (typically -0.15 percent/ $^{\circ}$ C) and if biased with PTAT emitter currents the base current, and thus any resistance-induced offset voltage, has the same TC as the junction offsets (which vary with kT/q). An adjustment made to null the composite offset at one temperature is therefore correct at all temperatures.

Q13 through Q16 are arranged in a thermally-symmetric quad to minimize the effect of temperature gradients generated by the high-power output stage of the V - F . All of the voltage gain is provided by Q14, which has the split-collector lateral p-n-p Q11 as the dominant load. This does not provide the highest gain configuration, but the scheme was used partly for simplicity and partly to achieve a good initial balance in the 5- μ A PTAT bias currents. A current balance of ± 1 percent is easily achieved in this way, whereas if separate p-n-p transistors with independent emitter resistors of 20 k Ω were used considerable chip area would be required to achieve the same matching.

To maintain a low temperature drift after nulling, the ratio of the bias currents for Q13 and Q14 must be temperature independent and the bias for Q17 must be equal to the sum of these, to preserve base-current cancellation. Fig. 6 shows a simple way to achieve this in a small area. A pair of auxiliary emitters are located in the base (epi pocket) of Q11/12 and connected through the external trim resistors to $+V_s$, to set up small correction currents. Since the same proportion of the injected current goes to Q12 as to Q11, the second-stage balance is maintained. Since both the main and auxiliary

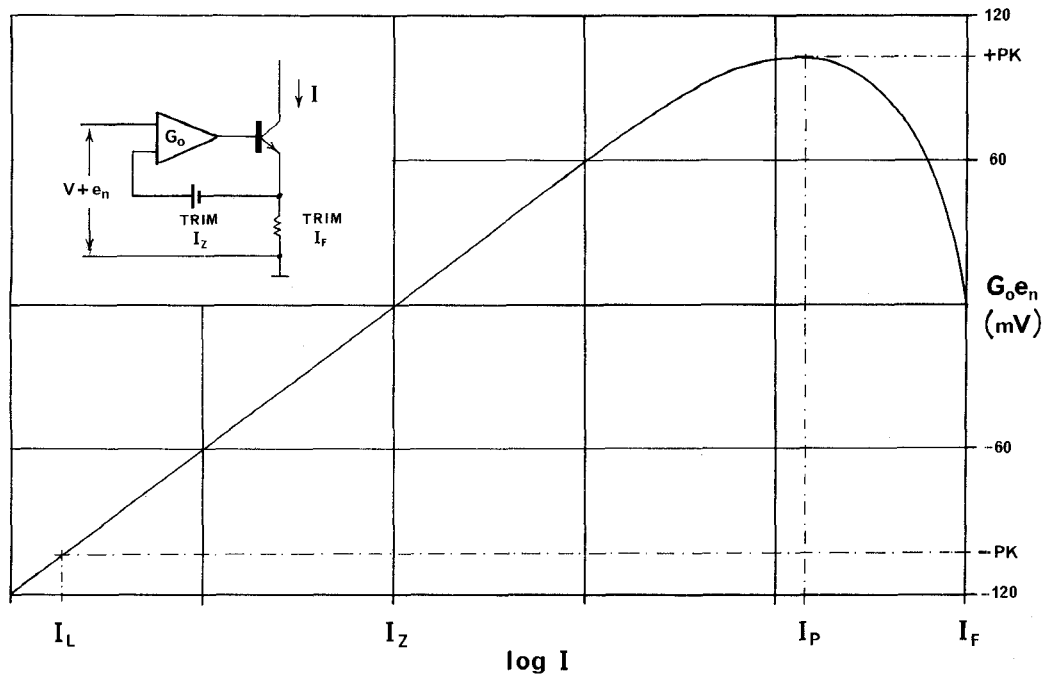


Fig. 5. Error voltage due to V_{be} of $Q47/48/49$. I_F is the FS current and I_Z the current at which the input offset is nulled.

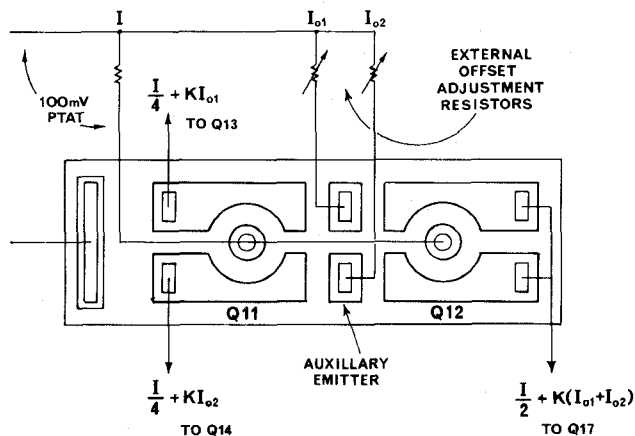


Fig. 6. Layout of $Q11/12$ showing auxiliary emitters.

currents are (very nearly) PTAT, ratios are maintained over temperature.

C. Intermediate Stage

$Q17$, $Q18$, and $Q19$ form a unity-gain buffer with a current gain of β^2 (because $Q17$ has its collector current forced by the local loop), and a further current gain of β is provided by $Q47/48/49$. Assuming a minimum β of 250 and a minimum value of $10\ \Omega$ for the scaling resistor ($10\ \text{mV FS}$), the input resistance at the base of $Q17$ is still more than $150\ \text{M}\Omega$ and the gain is unimpaired. $Q18$ serves to bootstrap the collector of $Q17$ and also keep its V_{ce} near zero (so improving the β matching with $Q13$ and $Q14$), while providing level shifting down to the base of $Q19$. HF feedforward around $Q18$ is provided by a 3-pF capacitor from the collector of $Q17$ to the

base of $Q19$, with a $100\text{-k}\Omega$ pinch resistor in the emitter of $Q18$; a small current source at the base of $Q19$ provides a charging current for this capacitor during slewing (not shown in Fig. 4).

The base-current drive to the output trio cannot exceed the nominal $10\ \mu\text{A}$ supplied by $Q12$. This provides the short-circuit protection at pin 3, since the maximum current is limited to β times $10\ \mu\text{A}$, which for a β range of 250 to 1000 corresponds to 2.5 to 10 mA. If $Q17$ were a simple emitter-follower additional protection circuitry would be needed.

V. REFERENCE GENERATOR

The reference voltage generator, Fig. 7, is based on Brokaw's cell [5]. The eight emitters of $Q7$ are of 1.3 mils diameter, while the single emitter of $Q8$ is of 1.4 mils diameter. The current-density ratio for equal collector currents is thus 6.90 which produces a ΔV_{be} of 50 mV at 300 K and allows the use of integrally-ratioed (hence, close-tolerance) resistors to generate exactly 600 mV at the emitter of $Q8$, half of which provides the $+1\ \text{mV/K}$ output. An even number of emitters in $Q7$ allows them to be laid out symmetrically with respect to $Q8$, to improve the ratio accuracy in the presence of processing and thermal gradients. The offset of 0.1 mil in the diameters can also be shown to mitigate the variation of output voltage which is due to the dependence on absolute V_{be} .

The voltage at the bases of $Q7$ and $Q8$ is nominally 1.212 V, which results in a zero TC at 300 K for $m = 1.27$ [5]. This is attenuated by $R7$ and $R8$ to provide a short-circuit proof 1.00-V output. These resistors also supply the primary reference current to the multivibrator, and are made up of integral

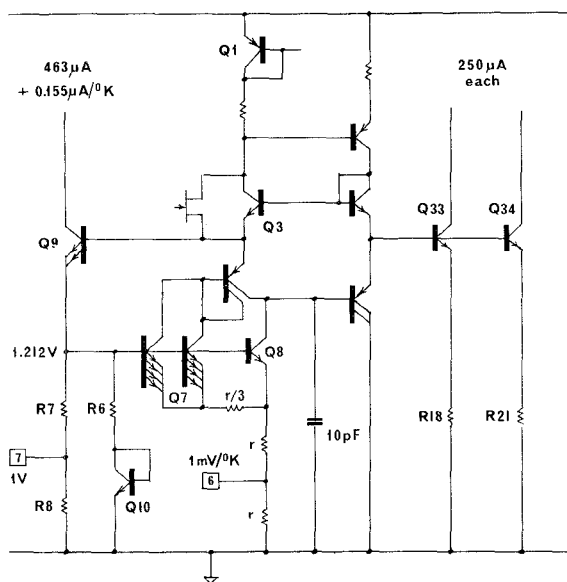


Fig. 7. Bandgap reference generator supplies fixed and PTAT bias currents.

units of 1.8 k Ω (to ensure good ratio accuracy with R14). The additional PTAT component of the composite reference current is provided by R6 and Q10.

Loading of the 1.00-V output will lower the oscillator frequency by constant proportion, without impairing the TC compensation, and external resistances down to 5 k Ω can be used with a correction to the scaling resistor. This allows the use of a variety of variable-resistance devices to be driven by the reference output. In many applications requiring a stable fixed frequency the 1.00-V output will be applied to the non-loading input, pin 5.

The two 250- μ A currents used to bias the inner emitter followers in the multivibrator are provided by Q33 and Q34. Their base currents cancel that of Q9, so preserving balance in the bandgap cell without unnecessary gain. An epi-FET provides startup; connected across Q3 it has little effect on the balance of the current mirror. HF compensation is provided by C1, using the design rules given in [5].

VI. OUTPUT STAGE

The utility of the V - F converter is enhanced by provision of a generous load-driving capability. High-current devices such as LED's (for optical coupling of the signal) and long cables can be driven. The circuit is shown in Fig. 8. Two output transistors, Q53 and Q54, are used to improve the thermal symmetry of the layout and lower the thermal resistance (under worst-case conditions the peak dissipation is 1 W). A low saturation voltage is provided by the use of devices similar in geometry to those described by Frederiksen and Howard [6]. Short-circuit protection is provided by a controlled base-current supplied independently to the two output transistors by the split-collector lateral p-n-p, Q51, which forms a differential pair with Q50. This driver stage operates at a current controlled by the pinch resistor R24, which has similar processing variations as beta. Consequently, the base drive is automatically adjusted to maintain a short-circuit

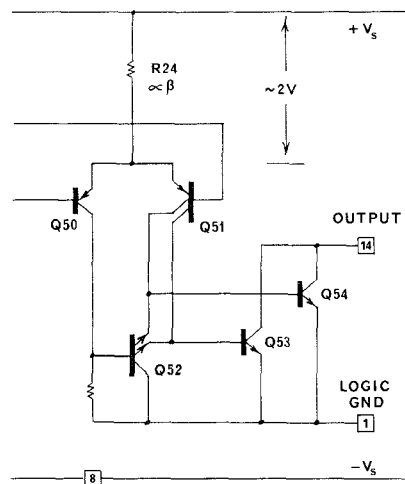


Fig. 8. The output stage. Q53 and Q54 are the large devices seen at the right of the photomicrograph (Fig. 9).

current which is reasonably independent of beta; a range from 30 to 40 mA is considered acceptable. The inverted transistor Q52 forms a cheap dual current mirror giving approximately equal turn-on and turn-off drive.

The output saturation voltage is typically 35 mV at 1 mA and less than 250 mV at 20 mA. Using a 500- Ω load the rise and fall times are 200 ns for a control current of 1 mA (FS frequency) rising to 1 μ s at 1 μ A. Note that several V - F converters can be multiplexed on to a common output bus using the emitters (pin 1) for chip selection.

VII. PERFORMANCE

The monolithic circuit is fabricated on a standard linear process with 1 k Ω /□ thin-film resistors. Laser trimming was considered, but since the scaling accuracy is determined by external timing components and a total system offset adjustment will be available, the advantage is marginal. Instead, several steps were taken to achieve a basically accurate product, including the use of integral-ratio photomatched resistors and emitters and a well-balanced layout. Fig. 9 is a chip photograph.

The performance is appraised in terms of the circuit's primary application of V - F conversion, for which the most important specification is linearity. Because there are many subtle sources of nonlinearity, the error does not have a consistent form over the dynamic range, except at high frequencies when the dominant error is due to switching-time delays. The best parts show less than ± 0.01 percent nonlinearity when used in the current-summing mode with an FS input of 10 V and a FS frequency of 10 kHz, and can be guaranteed to be less than ± 0.05 percent. Fig. 10 shows typical errors for 10 and 100-kHz FS ranges, the positive peak on the 100-kHz range being due to the fact that the circuit was trimmed at FS, where switching delays are already causing a reduction in frequency. The behavior for small inputs is dominated by offset, but it is noteworthy that a carefully-trimmed device con-

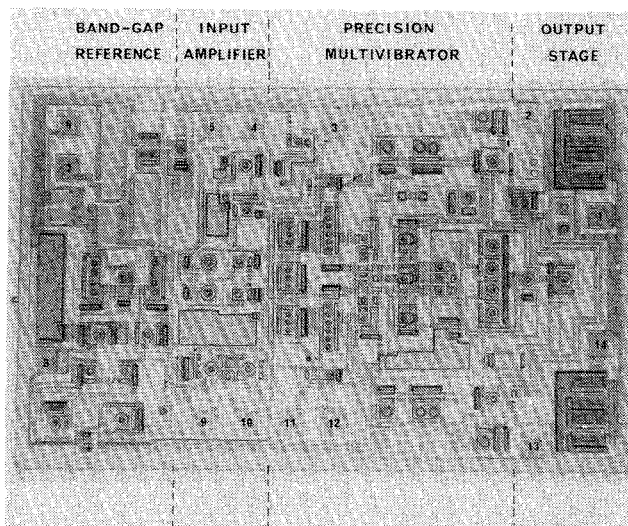
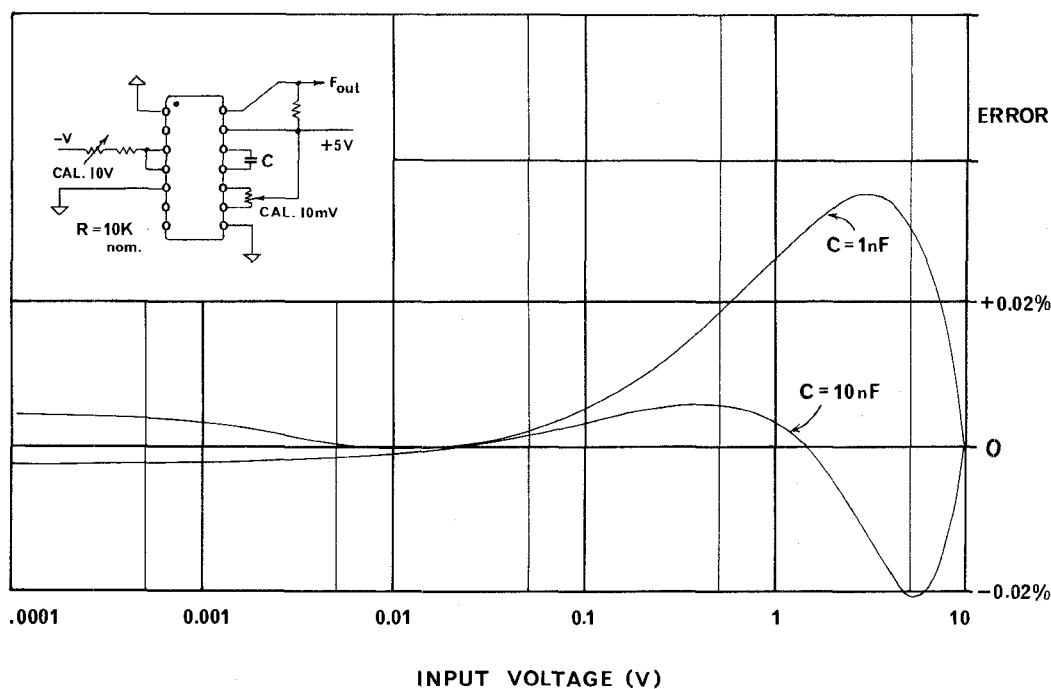
Fig. 9. Photomicrograph of the V - F converter.

Fig. 10. Typical nonlinearity showing operation over a 100 000:1 dynamic range.

tinues to oscillate below $100\ \mu\text{V}$ of input. The linearity in the voltage-follower mode is degraded by the beta variation with V_{ce} discussed in Section VI. Some samples show ± 0.03 percent nonlinearity but the average is about ± 0.06 percent, and can be guaranteed to be less than ± 0.1 percent for all ranges up to $100\ \text{kHz}$. The oscillator can be operated beyond $1\ \text{MHz}$, but the response of the output stage limits use to $200\ \text{kHz}$, where linearity is already less than desirable. The basic multivibrator will have the same high-frequency capabilities as any other emitter-timed circuit, the main contribution of this design being the accurate clamping arrangement and the temperature compensation.

Frequency drift over temperature was measured for 12

samples from two early production lots, and averaged $+70\ \text{ppm}/^\circ\text{C}$ at FS ($1\ \text{mA}$ control current, $f = 10\ \text{kHz}$), $+130\ \text{ppm}/^\circ\text{C}$ at one-tenth FS (equal to $+13\ \text{ppm}/^\circ\text{C}$ relative to FS), and $+150\ \text{ppm}/^\circ\text{C}$ at one-hundredth FS (equal to an insignificant $+1.5\ \text{ppm}/^\circ\text{C}$ relative to FS). The scatter of the TC's was about $\pm 30\ \text{ppm}/^\circ\text{C}$, and a small design trim has been made to center the distribution, which will provide an FS temperature-coefficient of less than $100\ \text{ppm}/^\circ\text{C}$ over the -55 to $+125^\circ\text{C}$ operating range.

Frequency stability with supply variations is typically $+100\ \text{ppm}$ per volt at FS, rising to $+1500\ \text{ppm}$ per volt at one-hundredth FS, which although undesirably high, is only $+15\ \text{ppm}$ per volt relative to FS. It is believed that this sensitivity

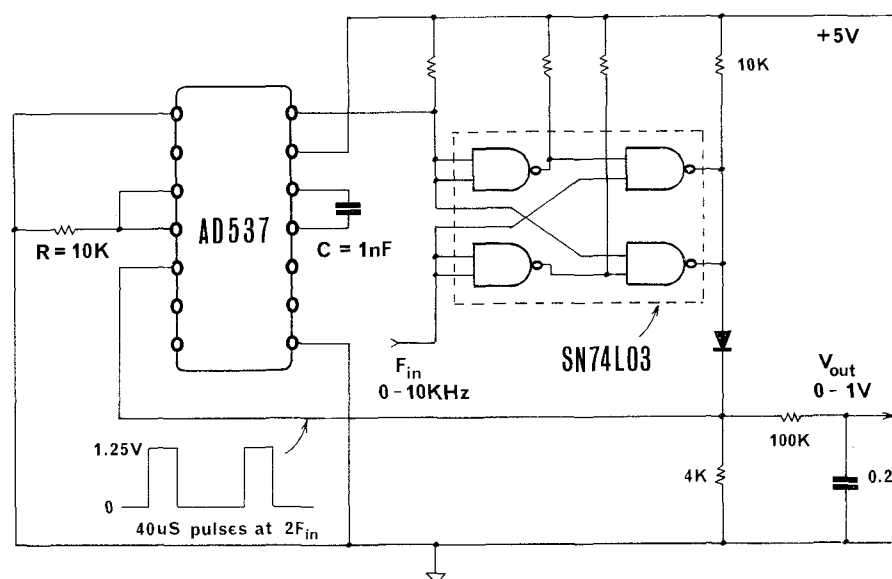


Fig. 11. Frequency-to-voltage converter. The circuit is a first-order precision phase-locked loop, using the quad-NAND gate as phase comparator.

is due to the design of the secondary current sources which use emitter-degeneration resistors (Fig. 3). These serve to improve rejection at FS, where the voltage across them is about 1 V, but are of no help down scale. This is also a contributing factor to nonlinearity.

The application of a $10\text{-}\Omega$ load between the output and $+V_s$ causes a peak dissipation of about 1 W for a supply of 30 V, and shifts the frequency by about -0.15 percent immediately, followed by a slow drift due to general chip heating. No significant effect on waveform symmetry is observable, evidence of the good thermal balance of the layout.

The drift performance of the interface amplifier is comparable with that of precision op amps. Initial offsets are less than ± 2 mV and after offset-nulling drifts of less than $1\text{ }\mu\text{V}/^\circ\text{C}$ are typical, with long-term drifts in the range 0.2 to $0.5\text{ }\mu\text{V}$ per week. Supply rejection is typically $20\text{ }\mu\text{V}$ per volt. Wide-band noise averages 15 nV per root-hertz. The input bias current is below $0.1\text{ }\mu\text{A}$, and the short-circuit limit on pin 3 is typically 7 mA.

Cycle-to-cycle jitter is less than ± 100 ppm, and can be reduced to ± 20 ppm using a decoupling capacitor from pin 2 to $+V_s$. General supply decoupling is also necessary in applications where timing jitter is critical, and the leads to the timing capacitor must be kept short to avoid induced noise voltages. The 1.00-V reference output shows a small spread of about ± 1 percent and has a typical TC of $-20\text{ ppm}/^\circ\text{C}$. The thermometer output is very linear (available measurement techniques were unable to reveal any curvature) over the range -30 to $+130^\circ\text{C}$, and the output is within ± 4 mV of nominal.

VIII. APPLICATIONS

The versatility of the circuit is impressive and many unusual applications have been found. For example, with the help of a

quad op amp and using the period control facility (pin 2) analog division of two variables can be performed, giving an output frequency proportional to the quotient with an error of less than ± 0.1 percent. The two applications described here demonstrate the usefulness of the square-wave output and the outputs on pins 6 and 7.

A. F - V Converter

Phase-locked loops are not generally used for precision F - V conversion because VCO's with adequate dynamic range and linearity have been hitherto unavailable, and the usual second-order loop has limited lock and capture range. Fig. 11 shows a first-order phase-locked loop that can lock to any frequency from zero to full scale, shown here as 10 kHz, with an over-range of about 10 percent. Signal acquisition occurs within a few cycles, so the response is determined mainly by the averaging filter; as in most F - V converters, this can either be a simple single-pole filter, as shown here, or it may be a more efficient multipole design. The circuit requires only a single $+5\text{-V}$ 4-mA supply and provides an output of $+1.00\text{ V}$ at 10 kHz.

A low-power TTL quad-NAND gate with open-collector outputs is used as the phase comparator, producing a positive pulse at the voltage input to the V - F converter having a lower level of exactly zero and an upper level of $+1.25\text{ V}$ (not critical). The V - F runs in a start-stop mode: when the input pulse is high a half-cycle of $40\text{ }\mu\text{s}$ is generated; when the pulse goes low the timing current drops to zero and the charge on the timing capacitor is held in readiness for the next half-cycle. The average value of the pulse is forced to equal that required to run the V - F at the input frequency. It is interesting to note that very high linearity can be achieved (typically ± 0.007 percent) even with a V - F converter having much poorer linearity! The explanation of this apparent paradox lies in the

fact that the V - F circuit operates at only one value of timing current (when the drive pulse is high) and behaves more like a monostable multivibrator dispensing fixed charge packets.

B. Two-Wire Centigrade Thermometer

The circuit can be used to convert ambient temperature to a frequency, simply by connecting the 1 mV/K output to the V - F input. This provides an absolute scale, and hence can convert temperatures below 0°C or 0°F . However, it may be useful to read temperature directly in a familiar scale, using a simple frequency-meter for the display. Of course, the scales then terminate at 0° , and the frequency becomes low near this temperature, so in many cases the absolute scale is preferable.

Fig. 12 shows how the offset is introduced, using the 1.00-V output. The component values shown are for the centigrade scale, requiring an offset of 273 mV, and include corrections for the loading effect (Section V). The frequency range is 0 to 1000 Hz for 0° to 100°C . Also shown is a method for conveying the output and the supply power over a single pair of conductors. The load resistance modulates the supply current at the output frequency, and this modulation is easily recovered at the supply end of the cable. Using a +5-V supply the self-heating effect due to 6.5 mW dissipation causes an offset of about $+1^\circ\text{C}$ in free-air conditions, which can be compensated if necessary by a slight adjustment to the 3-k Ω and 8-k Ω resistors.

IX. CONCLUSIONS

A V - F converter based on an accurate multivibrator has been described, having a dynamic range at least as high as a charge-dispensing converter, and a nonlinearity which is satisfactory for a large number of applications. A versatile input interface provides high sensitivity for either voltage or current inputs. The converter is complete with a stable voltage reference and can operate from a single supply. Several design improvements, notably in the secondary current sources, are planned, and there is a good prospect for achieving linearities of ± 0.02 percent or better on a production basis.

APPENDIX I

ANALYSIS OF MULTIVIBRATOR TEMPERATURE COEFFICIENT

Fig. 2 is used for analysis. The variable λ describes the modulation of the capacitor charging current λI . During most of the time λ is either 1 (current from left to right in capacitor) or -1 , but for a brief period preceding each switching phase, λ falls in value until a critical point $\lambda = \lambda_c$ is reached. There are four timing phases in a complete cycle.

Phase A: $Q1$ has just switched fully on, $Q2$ fully off, and $\lambda = 1$. This phase ends after a period t_A when the base-emitter junction of $Q2$ is exactly zero biased.

Phase B: $Q2$ begins to conduct, and $\lambda_c < \lambda < 1$. This has two effects: the capacitor charges progressively more slowly, and the collector clamping potentials shift. After a further period t_B the critical point $\lambda = \lambda_c$ is reached and the circuit switches regeneratively into Phase C.

Phase C: As Phase A, but with $Q1$ off, $Q2$ on, $\lambda = -1$.

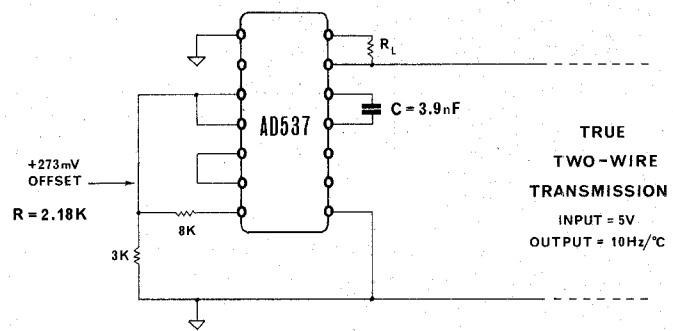


Fig. 12. Centigrade-reading temperature-to-frequency converter capable of operation at the remote end of a simple two-wire connection.

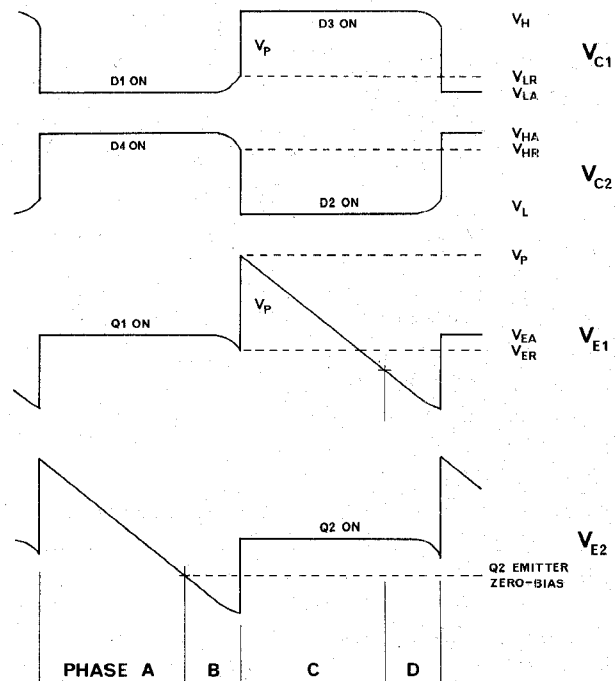


Fig. 13. Voltage waveforms of the multivibrator. The curvatures are exaggerated for clarity.

Phase D: As Phase B, but $-\lambda_c > \lambda > -1$, ending with $\lambda = -\lambda_c$, returning to Phase A.

Only the first two phases need be analyzed, the total period being $2(t_A + t_B)$. Fig. 13 shows the voltage waveforms, with some of the details exaggerated. The analysis is in four parts: determination of λ_c ; determination of voltages; duration of Phase A; duration of Phase B. The transistors are supposed to have no dynamic limitations, infinite beta, zero-ohmic emitter resistance, and equal junction areas. Although the last assumption is unnecessary (and in fact, untrue), it simplifies the analysis without invalidating it. The buffers $A1$ and $A2$ are assumed to have infinite current gain and introduce a level-shifting of E volts.

Determination of λ_c

The circuit enters regenerative switching when the loop gain reaches unity. This occurs when the sum of the collector load

resistances equals the sum of the emitter load resistances, using a small-signal analysis at this stage. This criterion is valid for reasonable time scales; at high frequencies the analysis would have to include dynamic factors which are beyond the scope of this discussion. The equation is

$$r_{e1} + r_{e2} = r_{c1} + r_{c2}. \quad (5)$$

During Phase B, $Q2$ is slowly turning on, and its emitter current is $(1 - \lambda)I$. Consequently, $r_{e2} = kT/qI(1 - \lambda)$. $Q1$ conducts $(1 + \lambda)I$, so $r_{e1} = kT/qI(1 + \lambda)$. The load resistance r_{c1} is generated by $D1$ (Fig. 2) conducting λI , and r_{c2} consists of $D4$ conducting λI , and $D5$ and $D6$ conducting $(2 - \lambda)I$, all in series. Therefore, the critical point occurs when

$$\frac{1}{1 - \lambda_c} + \frac{1}{1 + \lambda_c} = \frac{1}{\lambda_c} + \left[\frac{1}{\lambda_c} + \frac{2}{(2 - \lambda_c)} \right]. \quad (6)$$

This has the solution $\lambda_c = \pm\sqrt{3} - 1 = 0.732$ (the solution $\lambda_c = 2.73$ being inapplicable).

There is evidently a large current imbalance in $Q1$ and $Q2$ at the point of regeneration, so a temperature-proportional drift term will appear in the timing calculations.

Determination of Voltages

In the following, ϕ is used to denote the forward-biased junction voltage at a given temperature and at a current I to avoid confusion with V_{be} , which is not constant. At a constant temperature we can write $V_{be} = \phi + (kT/q) \ln(i/I)$, where i is a general current, and since all currents are related to I through the variable λ , the recurrent form $V_{be} = \phi + (kT/q) \ln f(\lambda)$ will appear.

With reference to Fig. 13 we can develop expressions for the important voltage levels. The "high" collector-clamping voltage is

$$V_H = -2 \left[\phi + \frac{kT}{q} \ln(2 - \lambda) \right] + \left[\phi + \frac{kT}{q} \ln \lambda \right]. \quad (7)$$

During Phase A, $\lambda = 1$ ($D4, D5$, and $D6$ all conduct I) so

$$V_{HA} = -\phi. \quad (8)$$

At the end of Phase B (brink of regeneration) $\lambda = \lambda_c$ so

$$V_{HR} = -\phi + \frac{kT}{q} \ln \frac{\lambda_c}{(2 - \lambda_c)^2}. \quad (9)$$

The general expression for the "low" collector-clamping voltage is

$$V_L = -V_R - \left(\phi + \frac{kT}{q} \ln \lambda \right). \quad (10)$$

During Phase A, $\lambda = 1$ ($D1$ conducts I), so

$$V_{LA} = -V_R - \phi. \quad (11)$$

At the end of Phase B, $\lambda = \lambda_c$, so

$$V_{LR} = -V_R - \phi - \frac{kT}{q} \ln \lambda_c. \quad (12)$$

To ascertain the voltage through which the capacitor must

charge we first find the emitter voltages at the beginning of Phase A and the end of Phase B. During these times the emitter of $Q1$ is at

$$V_E = V_H - E - \left[\phi + \frac{kT}{q} \ln(1 + \lambda) \right]. \quad (13)$$

For Phase A [using (8) and noting $\lambda = 1$]

$$V_{EA} = -E - 2\phi - \frac{kT}{q} \ln 2. \quad (14)$$

For Phase B, V_E can be calculated using (7). At the regenerative point

$$V_{ER} = -E - 2\phi - \frac{kT}{q} \ln \frac{(2 - \lambda_c)^2(1 + \lambda_c)}{\lambda_c}. \quad (15)$$

Now, the step labeled ΔV_p in Fig. 13 is simply $V_{HA} - V_{LR}$ and this step is transmitted to the emitter of $Q2$ during switching into Phase C. Thus the peak positive emitter voltage is

$$\begin{aligned} V_p &= V_{ER} + \Delta V_p \\ &= -E - 2\phi + V_R + \frac{kT}{q} \ln \frac{\lambda_c^2}{(2 - \lambda_c)^2(1 + \lambda_c)}. \end{aligned} \quad (16)$$

Duration of Phase A

The capacitor charges down from this potential until $Q2$ is zero biased. The base of $Q2$ is at $V_L - E$ at this instant, so the charging voltage during this phase is

$$V_A = V_p - (V_L - E) \quad (17)$$

$$= 2V_R - \phi + \frac{kT}{q} \ln \frac{\lambda_c^2}{(2 - \lambda_c)^2(1 + \lambda_c)}. \quad (18)$$

Consequently, the duration of Phase A is simply

$$t_A = \frac{C}{I} V_A. \quad (19)$$

By continuing in this way, the peak negative emitter voltage can be shown to be

$$V_N = V_{LR} - E - \left[\phi + \frac{kT}{q} \ln(1 - \lambda_c) \right] \quad (20)$$

and the total capacitor charging interval is

$$V_{TOT} = V_p + V_N = 2V_R + \frac{kT}{q} \ln \frac{\lambda_c^3}{(2 - \lambda_c)^2(1 + \lambda_c)}. \quad (21)$$

Thus, at absolute zero temperature the total time for all four phases is

$$t_{TOT} = 4 \frac{CV_R}{I} \quad (22)$$

which is consistent with the fact that at this temperature switching would occur abruptly, as assumed in the earlier analysis in this paper. In fact, proper allowance must be made for the gradual reduction in charging current during Phases B and D.

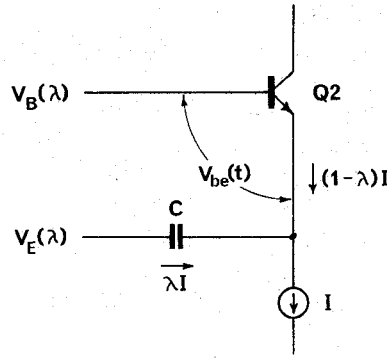


Fig. 14. Model for analysis of the transitional charging phase.

Duration of Phase B

Since the charging current is not constant during this phase (actually, during just a very small interval before regeneration) we must perform an integration. Fig. 14 shows the model for analysis of this phase. Note that there is a "moving target" in the sense that neither the base of $Q2$ nor the voltage at the "fixed" end of the capacitor is constant, and this must be included in the analysis. Using (10)

$$V_B(\lambda) = V_L - E = -V_R - \phi - \frac{kT}{q} \ln \lambda - E \quad (23)$$

and using (15)

$$V_E(\lambda) = -E - 2\phi - \frac{kT}{q} \ln \frac{(2 - \lambda_c)^2 (1 + \lambda_c)}{\lambda_c} \quad (24)$$

The constant terms E , V_R , and ϕ can be eliminated, since at the onset of Phase B the V_{be} of $Q2$ is zero and only the logarithmic variations due to λ are important. The V_{be} is therefore

$$V_{BE}(t) = V_B(\lambda) - V_E(\lambda) + \frac{I}{C} \int_0^{t_B} \lambda dt. \quad (25)$$

V_{be} can also be equated to the emitter current of $Q2$

$$V_{BE}(\lambda) = \frac{kT}{q} \ln \frac{(1 - \lambda)I}{I_s} \quad (26)$$

where

$$I_s = I \exp \left(-\frac{\phi q}{kT} \right). \quad (27)$$

We can thus make λ a function of V_{be}

$$\lambda = 1 - \frac{I_s}{I} \exp \left(\frac{V_{BE}(t)}{kT/q} \right). \quad (28)$$

Equation (25) is not amenable to a closed-form solution for t_B and the integration was mechanized for solution on a programmable calculator in the form

$$x = a(\lambda) + b \sum \lambda(x) \quad (29)$$

iterated until $\lambda = 0.732$, where

$$x = qV_{BE}(t)/kT$$

$$a(\lambda) = \ln \frac{(2 - \lambda)^2 (1 + \lambda)}{\lambda}$$

and

$$b = \frac{Iq}{CkT} \cdot \Delta t$$

with

$$x_0 = 0, \lambda_0 = 1.$$

Numerical values of $I = 100 \mu A$ and $C = 0.01 \mu F$ were used, with an initial time step, Δt , of $1 \mu s$ reducing to $10 ns$ for $\lambda < 0.932$. Confirmation of the small-signal analysis of the switching point was provided by the fact that λ changes rapidly beyond the critical value of 0.732 ; after several hundred iterations to reach this value a further eight were sufficient to change the sign of λ , corresponding to a reversal of current in the timing capacitor. This also suggests that the regenerative phase lasts for about $80 ns$ for the stated parameters.

Calculations

The periods t_A and t_B were calculated for $T = 150 K$ to $450 K$ in $50 K$ steps. An exact expression [7] for ϕ was used which includes the major temperature effects

$$\phi = E_{g0} \left(1 - \frac{T}{T_0} \right) + \frac{T}{T_0} \phi_0 - \frac{mkT}{q} \ln \frac{T}{T_0}. \quad (30)$$

The coefficient m was determined from previous work [5] related to achieving a nominally zero TC in a bandgap generator, and a median value of 1.25 was used. This value of ϕ is used directly in the calculation of t_A and provides I_s for the solution of t_B . A reference value of $\phi_0 = 650 mV$ at $T = 300 K$ and $100 \mu A$ was used.

The two sets of seven points were found by linear regression to accurately fit

$$t_A = 43.23 \mu s + 181.2 ns/K$$

and

$$t_B = 123.4 \mu s - 219.4 ns/K.$$

The total period is therefore

$$2(t_B + t_A) = 333.3 \mu s - 76.4 ns/K.$$

This result agrees exactly with the simplified theory at $T = 0$ K, and predicts a frequency drift of 230 ppm/K. This would be corrected by adding to the basic V_R of 833 mV a PTAT component of $+192 \mu\text{V/K}$. Measurements on the first prototypes show that this figure is insufficient, and a small correction was required to center the TC. The discrepancy can be attributed to an oversimplification of the model, which neglected transistor dynamics, ohmic resistance, and the effect of internal noise voltages. The latter could conceivably be responsible for an increased TC by causing the regeneration point to be earlier than predicted.

APPENDIX II

INPUT AMPLIFIER NONLINEARITY

The V_{be} of the trio Q47-49 varies logarithmically with the control current I , and introduces a nonlinearity which is reduced by the amplifier open-loop gain G_o , which appears at the input in addition to the linear term IR and a zero-adjust voltage E_z (injected using an external V_{os} potentiometer connected to pins 9 and 10). Thus

$$V = IR + E_z + \frac{kT}{qG_o} \ln \frac{I}{I_m} \quad (31)$$

where I_m is the FS value of I . Two adjustments are made to calibrate a V - F converter. First, the FS input voltage V_m is applied and the scaling resistor R adjusted for FS frequency f_m . Then a small voltage, typically one-thousandth of FS, is applied and E_z adjusted for correct frequency f_z . This process may need some iteration, but finally

$$R = \frac{1}{I_m} \left[V_m - \frac{kT}{qG_o} \ln \sigma \right] \quad (32)$$

and

$$E_z = \frac{kT}{qG_o} \ln \sigma \quad (33)$$

where $\sigma = f_m/f_z = I_m/I_z$. Using these expressions the input error voltage is found to be very nearly

$$e_n = \frac{kT}{qG_o} \left[\ln \frac{f}{f_z} - \frac{f}{f_m} \ln \sigma \right] \quad (34)$$

the peak value of this being

$$\hat{e}_n = \frac{kT}{qG_o} \left[\ln \frac{\sigma}{\ln \sigma} - 1 \right] \quad (35)$$

which occurs for $f_p = f_m/\ln \sigma$. Fig. 5 shows typical results.

At some current below I_z the input error will be equal in magnitude but opposite in sign to the value at f_p . This current is of interest, since it defines the total dynamic range for a given plus-minus error, and is given by

$$I_0 = I_z \exp \left[\ln \frac{\sigma}{\ln \sigma} - 1 \right]. \quad (36)$$

ACKNOWLEDGMENT

The author thanks L. Counts for his valuable assistance during the development of the monolithic circuit, P. Brokaw for the idea of using unequal emitter areas in the bandgap cell, and the staff of Analog Devices Semiconductor for their overall support of the development.

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