

SESSION X: Logic and Interface

THPM 10.3: A Super-Integrated 4-Decade Counter with Buffer Memory and D/A Output Converters

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USING A STANDARD BIPOLAR IC process, counting and memory circuits can be produced with high yield in an area typically only 5-10% of that required by prevalent structures. Using techniques to be described, eight MSI circuits and about 30 transistors were replaced by one 60 x 60 mil die containing four decade counters and associated memories, four decimal-analog converters (which provide the buffered output data in a form required by other parts of a system), and all the necessary input/output control circuits; Figure 1.

This area reduction is achieved primarily by combining as many devices as possible into common epitaxial regions, thus avoiding the need for wasteful isolation walls and spacings. In the die-layout of Figure 1, each of the four counter and memory units fits into one such region containing 30 NPN transistors, 20 triple-collector PNP transistors, 11 single-collector PNP transistors and 42 resistors in a stripe of 6 x 30 mils. Figure 2 shows in more detail the geometry of three stages of a single counter/memory unit.

Because of this commonality of elements, a secondary advantage results: the number of silicon-metal-silicon interconnects is greatly reduced. Data-flow proceeds very largely across lateral PNP bases or via buried-layer paths selectively diffused under the epi. For example, only 13 through-oxide connections are needed per stage compared to the 30 required using separately-isolated devices. This also reduces the area requirements (enlarged contact-areas in the diffusions are avoided), and significantly influences the compactness, yield and reliability of the total structure.

Such circuits are *super-integrated* in the sense that more efficient use is made of the distributed nature of planar circuits. It is frequently difficult to distinguish individual components, as Figure 2 will verify. In designing circuits this way, consideration is focussed on what can be achieved using advantageous geometries and the various semiconductor mechanisms, such as minority-carrier injection and collection, majority-carrier modulation, local field control, etc.

By putting geometry first, however, and removing the isolation walls between circuits, it becomes vital to choose circuit configurations that still behave predictably in the presence of large amounts of parasitic cross-talk. Figure 3 shows the three stages (of the ten in the ring) corresponding exactly to the area in Figure 2, with the important parasitic elements; the resistances between the PNP bases due to those parts of the epi not containing buried-layer. These are about 1,000 ohms for typical geometries on 6 μ , 1 Ω -cm epi. Notice that all the other resistors are base diffusions; these can also be in the same epi, since the latter is close to the V_c supply at all points.

The top half of Figure 3 is the memory, which we will temporarily assume is disabled by making $I_H = 0$. The counter clock lines ϕ_1 and ϕ_2 are driven alternately by a current I_H . Assume that stage N is active, and ϕ_1 is energized. I_H is picked up by the emitter of Q_7 and supplies base cur-

rent to Q_8 . For typical operating currents (0.3 to 3 mA) the h_{FE} of lateral PNP transistors of this geometry is low, particularly since the total collector current is shared among three partial collectors (and the substrate). Consequently, the voltage appearing across R_7 is small (typically 200 mV - 2 V) and Q_8 does not saturate.

Due to the parasitic epi paths, all the other PNP devices in this epi region also receive some of the collector current of Q_7 , the amount diminishing rapidly down the length of the stripe. These result in small currents in adjacent base resistors. In addition to this spurious current, R_6 receives a current equal to that in R_7 by virtue of a second collector of Q_7 making the base of Q_6 the most positive of the NPN transistors in the counter section. Thus, when the clock current is switched to ϕ_2 , it is Q_6 that picks it up, even though several of the bases may have been above the bias V_B . It is only necessary for the base of Q_6 to be more positive by a few tens of millivolts to ensure that I_H is regeneratively steered in Q_6 . The output to the buffer memory does not change significantly at this time, but the foregoing conditions have now shifted a half-stage to the right. A full count occurs when the current is restored to ϕ_1 ; the next buffer stage is then enabled.

When the current I_H is applied one of the bases, Q_5 , Q_{12} , Q_{18} , etc., will be most positive, depending on the counter state, and the count will be held in the corresponding buffer stage. The geometries are arranged so that the voltage across R_4 , R_8 , R_{12} , etc., due to buffer operation, is always greater than that from the counter output collectors. To prevent interference with the operation of the counter due to the

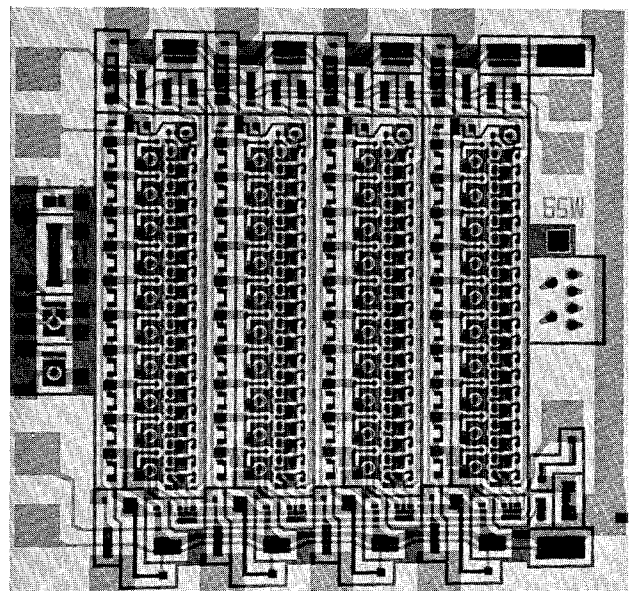


FIGURE 1—Photomicrograph of 60 x 60-mil die containing four decade counters, buffer memories and D/A converters; total, 196 NPN transistors, 124 PNP transistors and 215 resistors.

