

SESSION XIX: GENERAL PURPOSE ANALOG CIRCUITS

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FAM 19.1: An Analog Array Processor

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IN MANY IMAGING AND pattern-recognition fields, information is embedded in the *ratios* of the component signals in an array of concurrent signals, rather than in the *absolute magnitude* of individual signals. Such multi-channel signals often have a dynamic range of many decades, and some type of signal normalization is invariably required prior to subsequent signal processing (for example, A/D conversion) and feature-extraction.

To be described is a 16-channel analog array processor capable of performing realtime signal-normalization (and various other types of concurrent signal-processing in the amplitude domain). Figure 1 is a simplified schematic. Each of the sixteen inputs contributes *simultaneously* to each of the sixteen outputs. The (unipolar) input voltage range is from +10mV to +10V full-scale. The present device was fabricated on a standard junction-isolated bipolar process using diffused resistors; Figure 2. Quiescent power consumption is 1 to 2mW using the recommended $\pm 5V$ supplies.

Two modes of signal normalization are provided. In the first, the user sets the required full-scale output voltage using the input $W_{\max}$; the circuit automatically maintains *at least one output* to this value, and adjusts all other outputs *rationometrically* as determined by the input-array values. The function is thus

$$W_k = W_{\max} \frac{X_k}{\text{MAX}(X_k)}$$

where X_k is the voltage value of elements of the input array and W_k is the voltage value of the corresponding element of the output array. ($W_{\max}$ must be negative with respect to output common, so the circuit introduces an overall sign-inversion). An automatic tracking loop operates by sensing all sixteen outputs (using the vertical PNPs in Figure 1) and driving only one of these outputs to the set-point by dynamically controlling a bias current to maintain the demanded output amplitude.

In the second mode, an alternative input voltage Y is used to scale the outputs. In this mode the denominator becomes the *average* of all elements in the input array:

$$W_k = Y \frac{X_k}{\text{AVE}(X_k)}$$

¹Gilbert, B., "A New Wideband Amplifier Technique", Journal of Solid-State Circuits, Vol. SC-3, No. 4, p. 353-365; Dec., 1968.

²Gilbert, B., "Translinear Circuits: A Proposed Classification", Electronics Letters, Vol. 11, No. 1; Jan., 1975.

³Seevinck, E., "Analysis and Synthesis of Translinear Integrated Circuits", D.Sc Dissertation, University of Pretoria, South Africa; May, 1981.

In this mode the peak output will vary by a ratio of 16:1, since there may be only a single input present or all inputs may be equal; however, there are no tracking delays and the outputs rapidly follow variations in the input distribution. The circuit provides various other modes of operation, and with simple external circuitry may be used as a multi-channel multiplier or divider capable of processing *bipolar* input signals.

The core comprises a set of 32 bipolar transistors in a basic configuration which has been previously published¹ but not developed until now. Figure 3 shows the circuit in its simplest canonical realization. Input currents x_k are applied to diode-connected devices Qx_k and the total input current absorbed at a node (which in the practical circuit is the input of a 16:1 reduction current reflector, whose output is available as X_{ave}). The outputs appear at the collectors of transistors Qw_k . Their sum is constrained to be very nearly equal to the emitter source current I_w . Applying the translinear principle^{2,3} to this circuit, and making the usual assumptions of isothermal conditions and device ideality, the relationships shown in Figure 4 can easily be proven. It can be shown that it is not necessary for all devices to be strictly matched; it is only necessary that *pairs* of devices bear the same emitter-junction area-ratios and doping profiles. Thus, by providing access to the common lines the circuit can be extended without limit across package boundaries, using devices fabricated in different lots. The isothermal requirement remains, but the low dissipation of the circuit minimizes thermal problems.

The development of the idea (Figure 1) differs in two respects: the input devices Qx_k are operated in a forced-collector mode; a virtual-ground node is used, in conjunction with a resistor, to provide voltage-to-current conversion at the inputs. Opamps OA_k provide the needed gain. To minimize complexity, these are not fully-independent amplifiers, but share bias lines and one half of all input stages. HF feed-forward is used resulting in a bandwidth of approximately 1MHz (depending on input level) with bias current of about 2-4 μA per stage.

Figure 5 shows normalization using an input array of ten signals (unused inputs grounded) multiplexed left-to-right. In Figure 5a the inputs are shown at their reference level ($X_{\max} = +1.25V$); Figure 5b is a composite showing the outputs when all inputs are (i) at the reference level, (ii) reduced by a factor of 5 ($X_{\max} = +250mV$) and (iii) reduced a factor of 25 ($X_{\max} = +50mV$). The *pattern* of the output (sign-inverted for clarity) is seen to be essentially independent of the absolute magnitude of the inputs. Further design and layout improvements are being pursued to eliminate error sources; in particular, alterations to the cell design will improve channel-to-channel matching and alternative metalization methods will reduce errors from this source.

Acknowledgments

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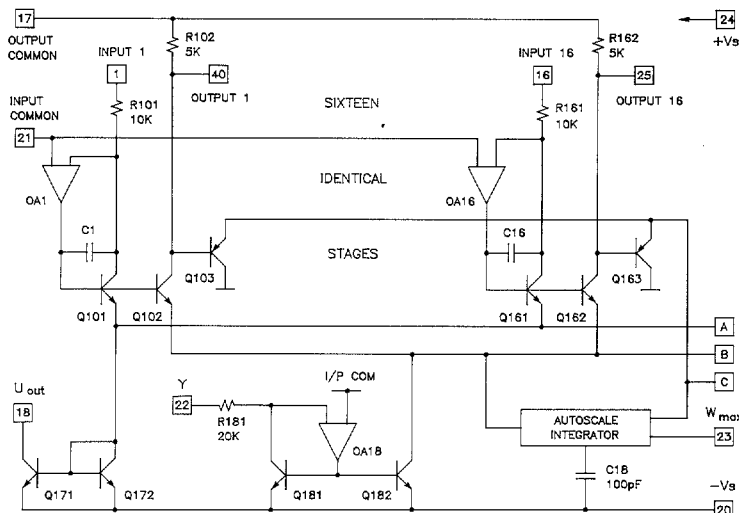


FIGURE 1—Simplified schematic of 16-channel analog array processor. A, B, C are expansion pins.

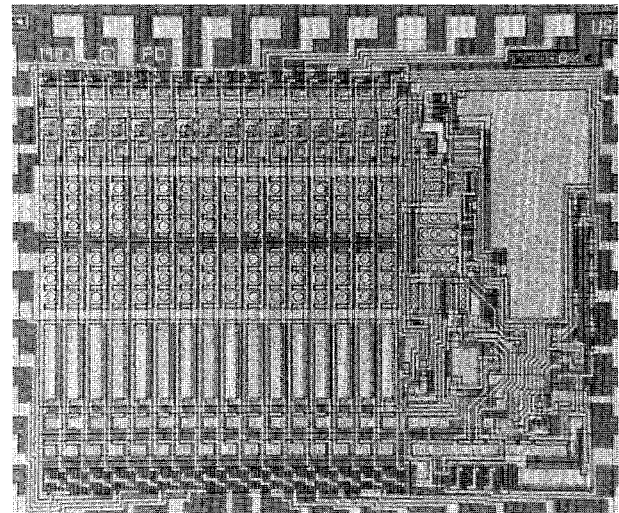


FIGURE 2—Chip photograph. Dimensions are 132 x 114 mils. Applying translinear principle to Figure 3:

$$\frac{x_1}{w_1} = \frac{x_k}{w_k} = \frac{x_N}{w_N}$$

However,

$$\frac{x_k}{w_k} = \frac{\sum x_k}{\sum w_k}$$

and

$$\sum w_k = I_w$$

Therefore

$$w_k = I_w \frac{x_k}{\sum x_k}$$

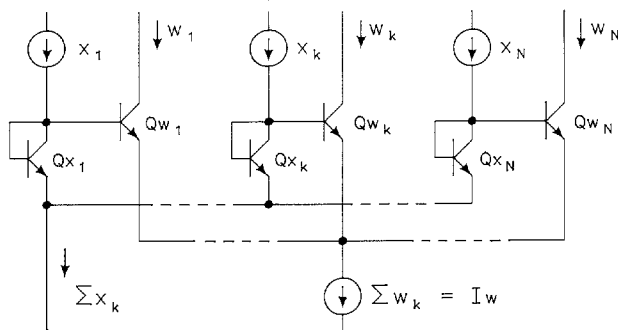


FIGURE 3—Rudimentary canonical form of processor.

FIGURE 4—Basic algebraic relationships.

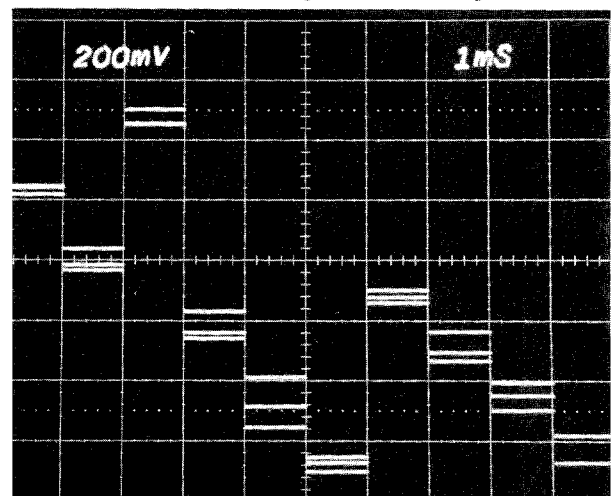
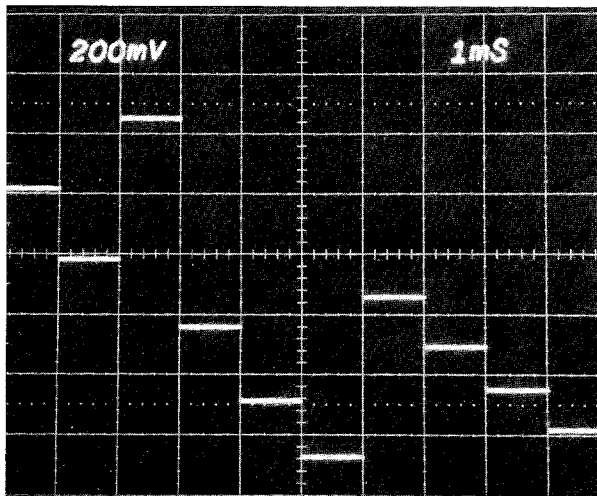


FIGURE 5—Input array/horizontal scan (a-left), output arrays for peak input levels of 1.25V, 0.25V and 0.05V — overlaid scans (b-right).