

References

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HIGH-ACCURACY VECTOR-DIFFERENCE AND VECTOR-SUM CIRCUITS

Indexing terms: Analogue-computer circuits, Summing circuits

By combining the exact nonlinear capabilities of translinear circuits with the high-gain, low-input-offset, load-driving and level-shifting properties of op-amps, analogue computing structures of great power and precision can be realised. This point is illustrated by circuits which compute the root sum of squares and root difference of squares.

Ashok has recently described¹ a 1-quadrant 'vector-difference' circuit using a direct translinear implementation of six transistors, to which the author added two further transistors to reduce the errors due to finite beta. It is suggested that the errors due to emitter-area mismatch are negligible, whereas, in fact, they become the limiting factor to accuracy in critical applications. Using his notation, the output current is

$$I_0^2 = K_1[I_1^2 + (1 - K_2)I_1I_2 - K_2I_2^2]^{\frac{1}{2}} \quad (1)$$

where

$$K_1 = A_5A_6/A_3A_4 \quad K_2 = A_2/A_1$$

and

$$A_k = \text{emitter area of transistor } Q_k$$

K_1 can be tolerated, since it causes only a linear, trimmable scale error; an equivalent error will arise in any translinear implementation. However, K_2 is more troublesome, since it will not, in general, be exactly unity and the unwanted product term will not be suppressed. Ashok's circuit is also rather difficult to drive in the usual case where inputs and output are voltages; the inputs are $2V_{be}$ s above ground and the output must be held close to the same potential to prevent errors due to the collector-base voltage-feedback effects into the emitter circuit of Q_5 .

This letter describes an alternative approach, requiring only four transistors in the translinear core, which is free from both beta and emitter-mismatch errors. Operational amplifiers are used to drive this core in conjunction with a resistor matrix. Now, matching of the resistors determines the suppression of the product terms, and this can be arbitrarily close. Of course, the price paid for adding amplifiers is mainly in response speed, since the direct translinear circuit can be quite fast, if the signals happen to already be in the form of currents. In practice, however, speed will always be determined by the supporting circuitry, and usually this will consist of operational amplifiers however the core is configured, particularly where the required precision is high.

This circuit has been used for computing vector difference and an allied operation, r.m.s.-d.c. conversion based on the difference of squares.² It is basically an accurate geometric-mean computer preceded by linear mixing of the two inputs. It is interesting to note that the same four transistors and four op-amps can be rearranged in scores of ways to realise all the major nonlinear analogue operations.

Fig. 1 shows the circuit broken down into four sections for clarity. The core can be seen by inspection to generate an output current of

$$I_0^2 = KI_aI_b \quad (2)$$

where

$$K = A_cA_d/A_aA_b$$

The output voltage is simply

$$V_0 = R_5(KI_aI_b)^{\frac{1}{2}} \quad (3)$$

and, if necessary, the scaling error due to the mismatch factor K can be eliminated by adjustment of R_5 . I_a and I_b are forced in the collectors of Q_a and Q_b by A_2 and A_3 ; hence beta errors are not experienced in the usual case where all betas are similar. All transistors operate with $V_{cb} = 0$; this condition is ensured for Q_b by the inclusion of the diode D_1 . D_2 and D_3 ensure predictable behaviour for reverse inputs, and standard compensation techniques³ are used (C and R) to stabilise the translinear loop.

When all resistors in the input matrix are equal,

$$I_a \propto V_1 + V_2 \quad I_b \propto V_1 - V_2 \quad (4)$$

and this condition is easily met using close-tolerance resistors. It is easily shown that to totally suppress the product term (cf. eqn. 1) a necessary condition is that

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} = \alpha \quad (\text{say}) \quad (5)$$

There is no necessity for $\alpha = 1$, and in some special applications, for example, in r.m.s.-d.c. conversion, where 'headroom' is required to accommodate input peaks, α may be manipulated to scale the V_2 input independently of the V_1 input:

$$V_0 = R_5 \left(\frac{K}{R_1R_3} (V_1^2 - \alpha V_2^2) \right)^{\frac{1}{2}} \quad (6)$$

The limiting errors in this circuit are now those incurred through the presence of finite ohmic resistance in the trans-

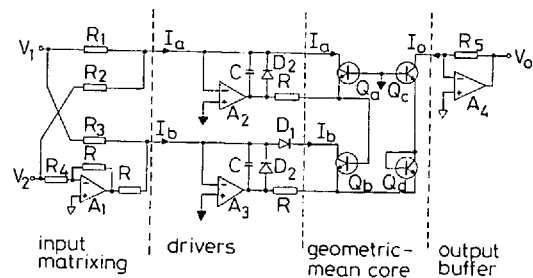


Fig. 1 Vector-difference circuit using geometric-mean 'core' and resistive input mixing

linear devices. However, using reasonable operating currents (< 1 mA) and preferably high-accuracy transistors, such as AD818 duals, resistive errors are fractional percent.

The circuit provides a bonus: the V_2 input can accept bipolar voltages with peak negative values of up to the same magnitude as V_1 . Thus, sine-to-cosine conversion can be performed without first generating the absolute value of the sine input.

To demonstrate the performance using inexpensive parts, the circuit was constructed using a CA3045 array, an RC4136 quad op-amp, equal input matrix resistors of $20 \text{ k}\Omega \pm 1\%$, $C = 30 \text{ pF}$, $R = 4.7 \text{ k}\Omega$. No adjustments were made to the circuit, but a small adjustment was needed to the amplitude symmetry of the sinusoidal V_2 input in the sine-to-cosine demonstrations shown in Fig. 2. This is because the effective gain of the circuit approaches infinity as V_2 approaches $\pm V_1$ and the output waveform is consequently very sensitive to minute amplitude imbalance on positive and negative peaks. Operation is shown for $f = 100 \text{ Hz}$ and inputs of 10 and 1 V; the output is still useful for inputs as small as 10 mV and at frequencies of at least 10 kHz.

Comment: Translinear circuits provide endless opportunities for the direct synthesis of multivariable nonlinear functions, often with great elegance and economy. However, their incompatibility with voltage interfaces (due, for example, to inputs and outputs being at elevated and imprecise potentials), their susceptibility to beta errors, and the generation of errors

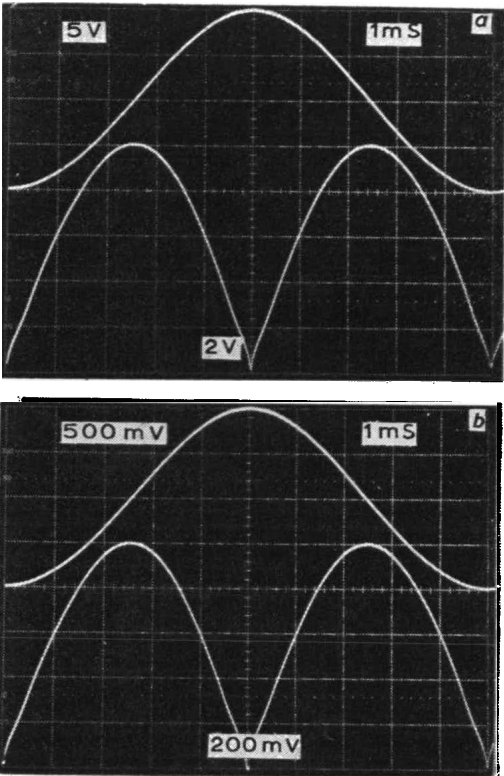


Fig. 2 Sine-to-cosine conversion using Fig. 1
Upper trace is input, lower trace is output. (a), $V_1 = +10\text{ V}$, $V_2 = 10 \sin 200\pi t$, (b) $V_1 = +1\text{ V}$, $V_2 = \sin 200\pi t$

due to emitter-area mismatch, which cannot be trimmed directly, all tend to reduce their practical value in the 'naked' form. The circuit in question is a good example of these problems.

On the other hand, by combining the functional flexibility of translinear circuits with the high-gain, low-input-offset, load-driving and level-shifting capabilities of op-amps, analogue computing structures of great power and precision can be realised. Economically, this approach is viable whether the system is built from 'discrete' parts (the cost of monolithic arrays of transistors and quad op-amps is now very low) or in monolithic form, where the op-amps may be very simple, special-purpose circuits, often containing less than ten transistors each. A further attraction of this approach is that it is usually possible to design the circuit so that any emitter-area mismatches which might cause scaling errors or unwanted nonlinearities can be absorbed by small adjustments to the associated resistors performing the voltage-to-current-to-voltage conversions. In a high-performance monolithic

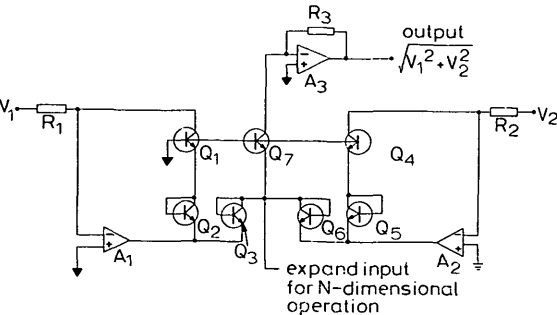


Fig. 3 Vector-sum circuit
Nominally, $R_1 = R_2 = R_3$ for unity scale factor. Any number of inputs may service the expand input, each requiring three transistors, an op-amp and a resistor

realisation this would be performed by laser wafer trimming, resulting in a low-cost product of very high accuracy.

A further example of this approach is shown in Fig. 3. This circuit performs 1-quadrant vector summation over many decades of voltage, and is easily extendable to any number of dimensions; a 3-dimensional summer requires only one quad op-amp and two 5-transistor arrays. Emitter-area mismatch can be shown to cause only minor scaling errors, easily removed by adjustment to the resistors; no crossproduct terms are generated. No errors are caused by finite, uniform beta, and beta mismatch can be absorbed by the resistors. The primary source of error is ohmic emitter resistance, but provided current densities are low (typically, fullscale input currents of $100\text{ }\mu\text{A}$ or less) overall nonlinearity can be maintained at well below 0.1%.

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DIGITAL FILTERS USING READ-ONLY MEMORIES

Indexing terms: Digital filters, Read-only storage
An algorithm, based on the replacement of multiply operations by table lookup, is presented for the computation of low-order digital convolutions.

Computation of an N -tap nonrecursive digital filter requires the evaluation of the discrete convolution

$$y_m = \sum_{n=0}^{N-1} a_n x_{m-n} \quad (1)$$

where $\{x_n\}$ is the input signal sequence, $\{y_m\}$ is the filtered signal sequence and $\{a_n\}$ is the N -point tap sequence. Direct calculation of eqn. 1 corresponds in the general case to N multiplications and $N-1$ additions per output sample. This processing workload can be reduced drastically if direct computation is replaced by a fast-Fourier-transform or number-theoretic-transform approach. In practice, however, transform techniques are not well adapted for implementation in small machines. In these cases, it is generally preferable to reduce the processing workload by resorting to various low-order convolution algorithms.¹⁻⁵ With the present trend towards large-scale integration and the rapid progress in the performance of read-only memory (r.o.m.) chips, it would be desirable to implement by table lookup the multiplications required for the evaluation of discrete convolutions.

Direct multiplication using table lookup usually leads to excessive r.o.m. sizes. R.O.M. size can be reduced at the expense of increased logic complexity by segmenting the input words.⁷ It is also possible to perform the multiplications by using logarithms implemented with read-only memories.⁶ Unfortunately, this last approach introduces inaccuracies.

In this letter, we shall propose the use of squaring to implement digital filters with r.o.m. and show that the number of table lookups can be reduced by low-order convolution algorithms. Using the conventional squaring approach, the discrete convolution can be computed by

$$y_m = \frac{1}{4} \left(\sum_{n=0}^{N-1} (a_n + x_{m-n})^2 - \sum_{n=0}^{N-1} (a_n - x_{m-n})^2 \right) \quad (2)$$