

A Monolithic Microsystem for Analog Synthesis of Trigonometric Functions and Their Inverses

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Abstract—A monolithic microsystem is described which provides direct analog synthesis of all trigonometric functions and their inverses. The new technique is based on the ratio of two sines, generated here by a novel sine-shaping network. The circuit offers high accuracy and bandwidth in an easily programmed 16-pin DIP.

I. INTRODUCTION

A MONOLITHIC circuit is described which generates *all* of the standard trigonometric functions (sine, cosine, tangent, secant, cosecant, and cotangent), their extensions (versine, coversine, haversine and exsecant), and their inverses (the most useful of which is the arctangent) in analog form. Formerly, separate techniques were needed for each function; in fact, only the sine, cosine, tangent, and arctangent have received serious attention. The key idea is the use of two identical sine/cosine networks connected to generate an output proportional to the *quotient* of their individual outputs. This new principle is presented in Section II.

Also novel is a sine/cosine network capable of fundamentally accurate synthesis over *arbitrarily large angular ranges* (for example, $\pm 500^\circ$). Section III describes this network and an exact expression for its output is derived in the Appendix. Prevalent networks are limited by the approximation technique and invariably capable of operation to only $\pm 90^\circ$. In this case, accuracy is limited mainly by the *quality* of the implementation.

Section IV describes a monolithic circuit¹ which realizes these principles and provides a *complete* solution to accurate trigonometric function synthesis at frequencies up to 1.5 MHz. The function is selected by pin strapping. Preprogrammed amplitudes can be digitally selected or an external amplitude-control voltage used. Operating conditions resulting in invalid outputs (for example, calling for $\tan 90^\circ$) can be trapped by on-chip circuitry which sets the output to zero and flags the error condition. The performance of this circuit is reviewed in Section V.

II. UNIVERSAL TRIGONOMETRIC-FUNCTION BUILDING BLOCK

The synthesis of the sine function using analog techniques has long been of interest because sine-shaping networks can be used to generate continuous sine wave signals when driven by a triangular wave. Sine circuits are also used in analog computa-

tion applications, such as polar-to-rectangular conversion (vector resolution), in which case the cosine function is also needed. A network having the ability to respond accurately over a *wide* angular range can be used for either sine or cosine generation, these functions differing by only 90° . A recent paper [1] describes a translinear [2] circuit which generates the cosine from -180° to $+180^\circ$, and can provide good spectral purity as a triwave-to-sine converter when fully trimmed.

The tangent and its inverse, the arctangent, are useful in some scanning systems and in rectangular-to-polar conversion (vector composition). Representative techniques can be found in [3] and [4], and some useful approximation formulas are given in [5]. The remaining functions (secant, cosecant, and cotangent) and their inverses appear to be of little practical importance. Nevertheless, there would be considerable advantage in a simple technique capable of generating *all* trigonometric functions with equal facility, particularly if it afforded high accuracy, wide angular range, and high speed. This paper shows that such a technique exists, and is eminently practical in a monolithic realization.

A. Universal Synthesis Technique

All the standard trigonometric functions can be expressed as the *quotient of two sines* when the argument of each represents the *difference* of two angles, one of which in each case is either 90° or 0° (Table I). At first, it may seem that this approach requires two independent sine-function circuits, followed by an analog divider; Fig. 1(a) shows a scheme that avoids this complexity. The sine-shaping networks are differential transconductance elements, having a differential input voltage representing angle and a control current input (I_E) to which the differential current output (shown here in single-sided form for clarity) is exactly proportional. Thus

$$I_Z = \eta I_E \sin(x_1 - x_2) \quad (1)$$

$$I_A = \eta I_E \sin(y_1 - y_2) \quad (2)$$

where η is a constant of proportionality (the network *efficiency*) and the angles x_1, x_2, y_1 , and y_2 are proportional to the corresponding input voltage. For example, $x_1 = X_1/V_s$, where X_1 is the angle voltage and V_s is the *angular scaling voltage*. A major consideration in any practical system is that V_s be precise and stable.

The *control op amp* forces a balance between I_A and the current due to the amplitude control input, V_A , by varying I_E

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¹ Analog Devices AD639.

TABLE I

$\sin(z) = \frac{\sin(z-0)}{\sin(90-0)}$	$\operatorname{cosec}(z) = \frac{\sin(90-0)}{\sin(z-0)}$
$\cos(z) = \frac{\sin(90-z)}{\sin(90-0)}$	$\sec(z) = \frac{\sin(90-0)}{\sin(90-z)}$
$\tan(z) = \frac{\sin(z-0)}{\sin(90-z)}$	$\cot(z) = \frac{\sin(90-z)}{\sin(z-0)}$

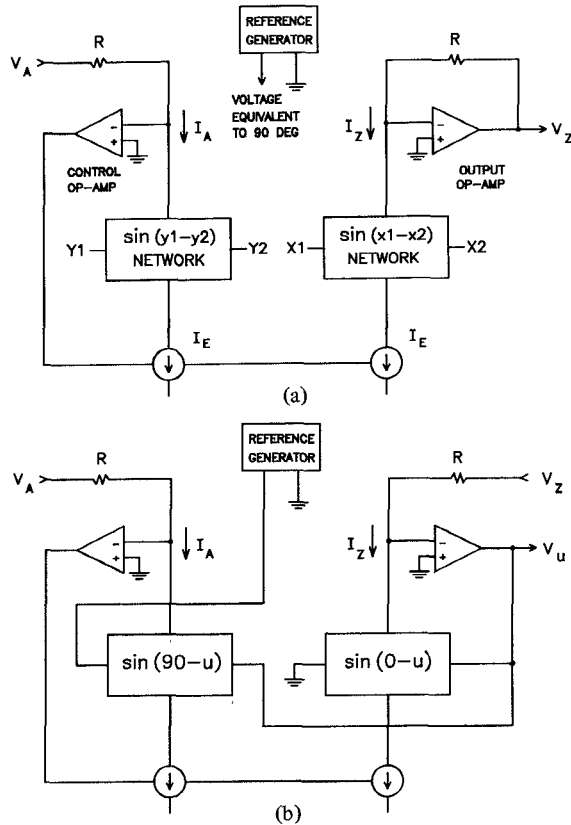


Fig. 1. (a) Universal trigonometric function generator;

$$V_Z = V_A \sin(x_1 - x_2) / \sin(y_1 - y_2).$$

(b) Typical inverse mode (arctangent) uses feedback to the angle inputs.

which thus becomes a function of both V_A and the angles y_1 and y_2 as follows:

$$I_E = \frac{V_A}{R} \frac{1}{\eta \sin(y_1 - y_2)}. \quad (3)$$

The *output op amp* converts the current I_Z generated by the right-hand network to the output voltage V_Z . Thus

$$V_Z = V_A \frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)}. \quad (4)$$

Consideration of the behavior of the control loop shows that the feedback will become positive, and control will be lost,

when $\sin(y)$ is negative. It follows that y is constrained to the ranges

$$2n\pi \leq y \leq (2n+1)\pi \quad (5)$$

where n is integral. From this constraint it follows that $I_A \geq 0$ so the amplitude control voltage V_A must be positive.

I_E becomes large as $\sin(y)$ approaches zero, and there will be a practical limit beyond which the network will fail to operate correctly, so further constraints need to be placed on y . The complete circuit detects conditions such as this, and warns the user by generating a digital flag output.

The practical building block is completed by the addition of a stable reference generator whose +1.8 V output corresponds to an angle of 90° , using a scaling of 20 mV per degree. Two full "revolutions," from -360° to $+360^\circ$, require a differential input of ± 7.2 V, well within the capability of typical sources.

B. Synthesis of Inverse and Offset Functions

The *inverse* of a nonlinear function can be generated by including the function in a feedback path around an operational amplifier. Fig. 1(b) illustrates how the universal trigonometric building block can be configured to generate the arctangent, as an example.

First, note that the angle connections are set up to $-\tan(u)$, (ensuring negative feedback) using the relationship

$$-\tan u = -\frac{\sin(u)}{\cos(u)} = \frac{\sin(-u)}{\cos(u)} = \frac{\sin(0-u)}{\sin(90-u)}. \quad (6)$$

The voltage corresponding to angle u is forced by the output op amp, by balancing the equation

$$\frac{V_Z}{R} = \frac{V_A}{R} \{-\tan(u)\}. \quad (7)$$

It follows that

$$u = \arctan \left\{ -\frac{V_Z}{V_A} \right\}. \quad (8)$$

(The monolithic circuit provides differential inputs for both A and Z , so the negative sign can be eliminated in practice.) All other inverse functions can be generated in a similar way.

Certain applications require the use of extensions to the standard functions, generated by the use of an offset term. These are 1) the versine, $\text{vers}(x) = 1 - \cos(x)$; 2) the coversine, $\text{covers}(x) = 1 - \sin(x)$; 3) the haversine, $\text{hav}(x) = \frac{1}{2} \text{vers}(x)$; and 4) the exsecant, $\text{exsec}(x) = \sec(x) - 1$. The monolithic circuit allows the addition of an offset of essentially any amplitude to the output function, with a unity scale factor. Since the amplitude control also provides unity gain, and either sign of each function can be generated, it is a simple matter to couple these two inputs and maintain correct proportioning to the composite function for all amplitudes.

III. SINE-SHAPING NETWORKS

Sine-shaping techniques fall into the following three categories:

- 1) Linear-segment approximations.
- 2) Continuous-function synthesis using algebraic approximations.
- 3) Continuous-function synthesis using circuits based on bipolar differential pairs.

A good summary of the well-established linear-segment approach is provided by Evans and Schiffer [6], who provide useful tables of breakpoint locations and both analytic and empirical formulas for calculating total harmonic distortion. This approach is often implemented with diode-shaping networks of various kinds [7], [8].

Many algebraic approximations have been published including those using analog multipliers [9], nonintegral power terms [3], and translinear circuits [1], [2]. Some of these approximations are theoretically capable of close conformance to the sine over narrow angular ranges.

In the third category, Grebene [10] seems to have been the first to have based a sine shaper on the hyperbolic tangent transconductance of a bipolar differential pair. This approach has been analyzed by Meyer *et al.* [11] and is attractive because of its simplicity, particularly in a low-cost monolithic realization. The accuracy of the basic circuit can be improved by adding some of the angle input directly to the output; the distortion of this approach has been analyzed by Evans and Schiffer [12]. Unfortunately, the angular scaling factor of these circuits is strongly temperature-dependent and the angular range is usually restricted to $\pm 90^\circ$.

A. Sine Synthesis Over Large Angular Ranges

Gilbert [13] has devised a sine-synthesis technique based on the use of a *multiplicity* of differential pairs, having their outputs connected in alternating antiphase [Fig. 2(a)]. This technique possesses the following three unique properties:

- 1) The output function theoretically exhibits astonishingly small error for circuits of modest complexity, and can be shown to *vanish* completely in a limiting case; the technique thus closely approaches *exact* sine synthesis. Accuracy in practice will be limited largely by the *quality* of the devices, particularly V_{BE} matching.
- 2) Synthesis can be continuous over *any angular range*: each stage adds a further π radians. The circuit shown, for example, provides $\pm 360^\circ$ of range.
- 3) The angular scaling is *precise* and *temperature-stable*: the zero crossings of the function occur at exactly $\pm nE_B$, where n is integral and $E_B = IR$ is typically 75 mV.

This circuit also provides linear control of output amplitude by varying the currents I_E . The *efficiency* (the ratio of the sine output amplitude to the total emitter supply current) is a strong function of temperature; however, when two identical networks are used in a *ratiometric* configuration (Fig. 1) the amplitude is temperature-compensated. A more serious disadvantage is that this efficiency is quite low, and decreases as the angular range is increased by the addition of stages because for a given angle most stages are fully switched and contribute only to the *common-mode* output current. For the circuit shown, only 6 percent of the total emitter current supply is

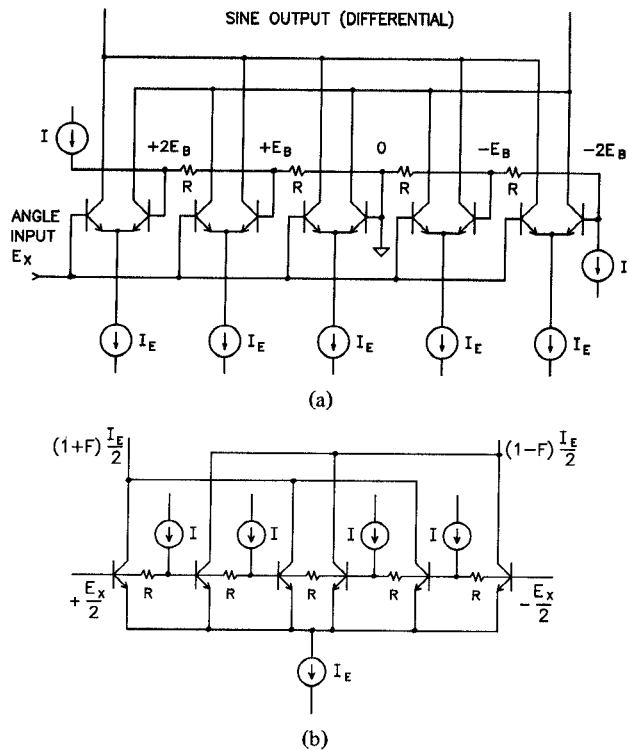


Fig. 2. (a) A sine shaper having precise scaling and an angular range of $\pm 360^\circ$. (b) New circuit is simpler and has higher efficiency (5 times in this case).

usable (differential) output at 300 K, dropping to about 3 percent at 400 K. Furthermore, the circuit requires a multiplicity of current sources, mismatches which introduce error.

B. A New Sine-Shaping Circuit

The new technique bears a close similarity to the one just described. Fig. 2(b) shows a circuit having all its advantages and:

- 4) Only a *single* current-source I_E is required; the output is still directly proportional to this current.
- 5) The transfer efficiency is now independent of the number of stages and is typically 36 percent at 27°C .
- 6) Each additional π radians of angular range requires the addition of only *one* transistor, not a pair.

The general network consists of N identical ideal bipolar transistors, $N - 1$ equal resistors of value R , and $N - 2$ equal current sources of value I . Our discussion will assume n-p-n transistors, in which case the bias currents I flow *toward* the network. N may be as small as 4 and as large as desired; it is usually even, resulting in an overall function which has odd-order symmetry.

The ends of the resistor string are driven by voltage sources, either differentially or from one side only. Let the total voltage across the string be E_x ; this voltage controls the instantaneous *equivalent angle* of the generated function, and over the region of the function for which it closely approximates the sine, the angle is *proportional* to this voltage. The bias voltage, $E_B = IR$, determines the angular scaling factor. The Appendix shows that the output undergoes one complete

cycle (2π radians) for an interval of $2(N-1)E_B$ in the voltage E_x ; that is

$$\text{equivalent angular input (radians)} = x = \frac{\pi E_x}{(N-1)E_B}. \quad (9)$$

The scaling can thus be accurate and temperature stable, since it is a simple matter to ratio E_B to a precision reference voltage. The output function exhibits $(N-1)$ zero crossings and is valid over a total range of $(N-2)\pi$ radians.

A key parameter is the *bias factor*, α , defined (see the Appendix) as

$$\alpha = \frac{E_B}{kT/q}. \quad (10)$$

It determines both the error (deviation of the normalized sine from an ideal unit sine) and the efficiency of the network. It can be shown that for a circuit containing a very large number of transistors, the peak error approaches

$$\epsilon = \sqrt{2} \exp \left\{ \frac{-2\pi^2}{\alpha} \right\} \quad (11)$$

and the efficiency

$$\eta = 2 \exp \left\{ -\frac{\pi^2}{2\alpha} \right\}. \quad (12)$$

As we shall see, the minimax error can actually be much less than (11) predicts. However, inserting a representative value of $\alpha = 2.9$ yields $\epsilon = 0.00156$ (0.16 percent) and $\eta = 0.3648$ (36.48 percent). Fig. 3 plots ϵ and η , from which it is immediately apparent that while the error can become extremely small as α diminishes, it is at the cost of efficiency. Furthermore, since α is inversely proportional to absolute temperature, it follows that both of these figures are strongly temperature-dependent. The temperature dependency of the efficiency is tolerable in the ratiometric scheme described earlier, but the variation in the error may be troublesome. In practice, this calls for judicious choice of the bias factor.

We will now examine the theoretical performance of sine shapers using practically sized networks, having N between 4 and 10.

C. Four-Transistor Circuit

Fig. 4 shows the simplest realization, having $N = 4$. The output modulation factor is

$$F(E_x, E_B) = \eta \sin \frac{\pi E_x}{3E_B} \quad (13a)$$

where the efficiency η is given by (12). Although not much more complex than the simple differential pair, this circuit provides accurate angular scaling, low error for equivalent angles of magnitude up to 90° , and a range of more than $\pm 180^\circ$ over which the function is sensibly sinusoidal.

Consideration of the physical behavior for a typical E_B of 75 mV ($\alpha = 2.9$ at 27°C) is helpful. When $E_x = 0$, the network is completely balanced: regardless of the magnitudes of E_B and I_E the net output is zero. Specifically, the inner bases are 75 mV more positive than the outer bases, so nearly 95 per-

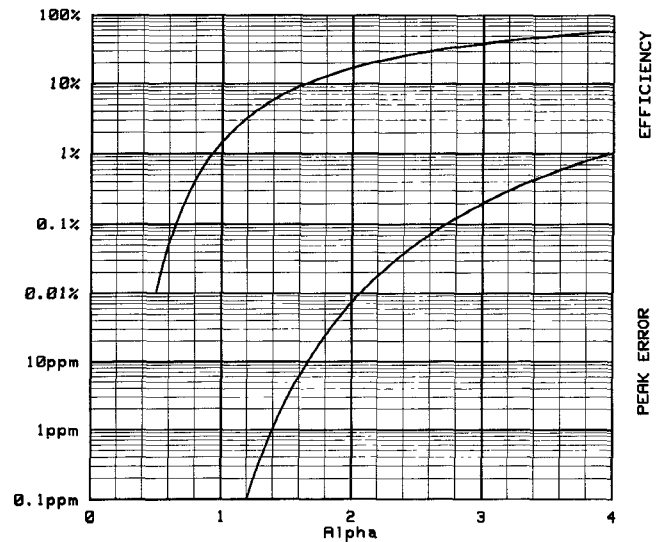


Fig. 3. Lower curve: peak error over $\pm 90^\circ$ versus the bias factor $\alpha = IR/(kT/q)$. Upper curve: network efficiency declines rapidly as α is reduced, so a compromise α is necessary.

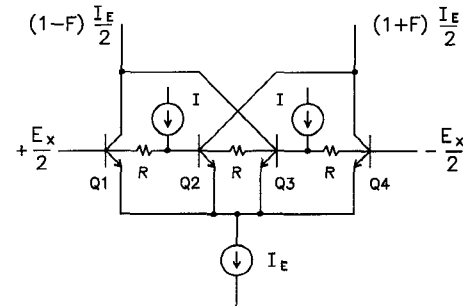


Fig. 4. Simplest form of new sine-shaping network has useful range of $\pm 180^\circ$ and theoretical errors below 0.01 percent under optimum conditions.

cent of I_E flows in $Q3$ and $Q4$. When $E_x = 112.5$ mV ($=3E_B/2$, the design value for 90°) the base of $Q3$ becomes 37.5 mV more positive than its neighbors, and 67.9 percent of I_E flows into $Q3$, 16 percent into each of $Q2$ and $Q4$, and only 0.1 percent into $Q1$; the net differential output is thus $0.36I_E$. When $E_x = 225$ mV ($=3E_B$) the bases of $Q3$ and $Q4$ are at the same potential, and 75 mV more positive than $Q2$. Now, 48.7 percent of I_E flows in these transistors, and only 2.6 percent in $Q2$, while $Q1$ is virtually cut off. The balance is now not perfect due to the finiteness of the network, and the net output is $0.016I_E$.

Closer evaluation shows that the minimax ($\pm 90^\circ$) error for $\alpha = 2.9$ is ± 0.32 percent and this is the smallest possible error when using exact scaling. Fig. 5(a) shows the error computed using the exact expression derived in the Appendix; it is mostly in the form of second harmonic. Interestingly, much lower error is possible by slightly altering the angular scaling. Fig. 5(b) shows the optimum which occurs when $\alpha = 2.66$ and the scaling is adjusted by about 0.7 percent, the minimax error is now only ± 0.008 percent. However, for a fixed E_B the bias factor α is temperature-dependent, and hence these optima cannot be held over temperature. (E_B could be rendered proportional to absolute temperature (PTAT), in which case a

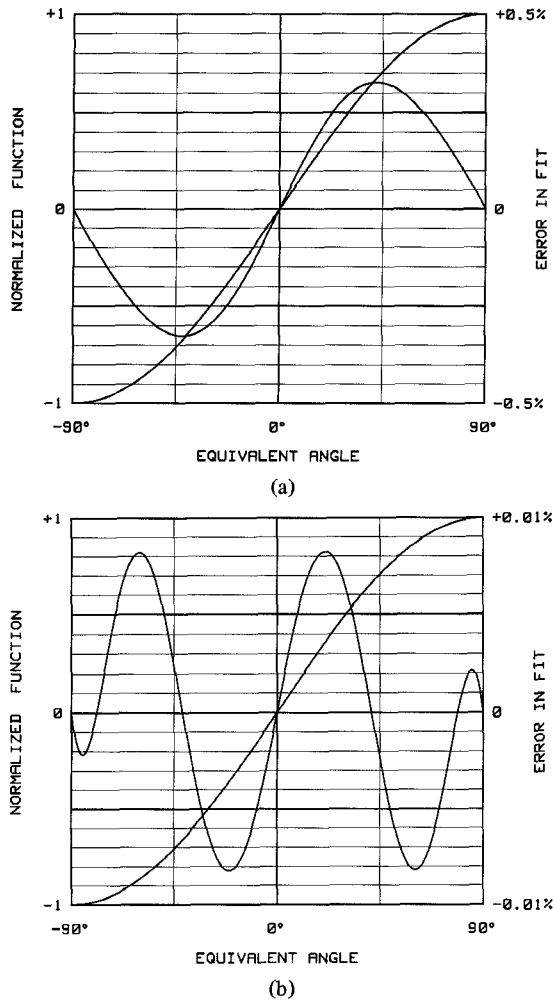


Fig. 5. The normalized output and instantaneous error for the four-transistor circuit: (a) using $\alpha = 2.9$; (b) see text.

temperature-compensated input attenuator would be required, as is the case for the networks described in [10]–[12].)

D. Higher-Order Circuits

When $N = 6$ the output modulation index is

$$F(E_x, E_B) = \eta \sin \frac{\pi E_x}{5 E_B}. \quad (13b)$$

Fig. 6 shows the function for $E_B = 75$ mV and $T = -55^\circ\text{C}$, 25°C , and $+125^\circ\text{C}$, and the strong temperature dependence of amplitude is apparent. The theoretical minimax ($\pm 90^\circ$) error of ± 0.006 percent occurs for $\alpha = 2.145$. However, since the efficiency at this value of α is only 20 percent, and in practice the risk of further errors due to component mismatches must be considered, these being more troublesome as the efficiency is lowered, a larger value is likely to result in lower net error.

Fig. 7(a)–(c) shows the magnitude of the instantaneous error for the six-transistor circuit at three different temperatures, and with $E_B = 75$ mV. A logarithmic scale is used to accommodate the wide range of magnitudes; only positive angles are shown, but of course the errors are symmetrical. At room temperature [Fig. 7(b)] the peak error within the central $\pm 90^\circ$ is 0.16 percent, computed using the exact expression (A9), in excellent agreement with the value predicted by (11),

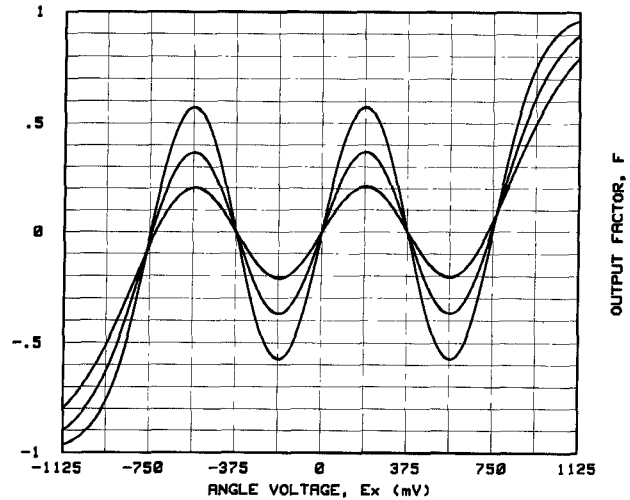


Fig. 6. Output of the six-transistor network, showing temperature dependence: $E_B = 75$ mV.

and remains under 0.2 percent to beyond $\pm 250^\circ$, after which it rapidly worsens. At -55°C the error at small angles exceeds 1 percent [Fig. 7(a)], but remains at this level to nearly $\pm 360^\circ$, while at $+125^\circ\text{C}$ [Fig. 7(c)] the error within the central $\pm 90^\circ$ is only slightly more than 0.01 percent, increasing to 0.3 percent at 180° .

These curves show that there is no truly optimum choice of α for a circuit intended to operate over a wide temperature range, and that accurate performance to $\pm 360^\circ$ necessitates the use of more than six transistors.

Fig. 7(d)–(f) shows the corresponding curves for $N = 8$, using the same bias voltage. As would be expected, the behavior in the central $\pm 90^\circ$ is essentially unaffected, but now the room-temperature error is maintained below 0.2 percent as far out as $\pm 430^\circ$, and even at the temperature extremes the error out to $\pm 360^\circ$ is tolerable (0.3 percent at 125°C , 1.1 percent at -55°C).

As was the case for $N = 4$, a considerable improvement in error within $\pm 90^\circ$ can be achieved using a slight adjustment to the scaling. It can be shown that the minimax ($\pm 90^\circ$) error can be theoretically as low as 2 parts per million.

Extensive numerical analyses using (A9) have been made to fully map out the capabilities of these circuits. Fig. 8, for example, shows the peak error for $N = 4$ to 12 as a function of α . For $N = 12$ with scaling adjustment the minimax ($\pm 90^\circ$) error can be as low as 3 parts per billion. It is interesting to note that for $N = 4, 8, 12 \dots$ the minimum-error region is rounded and lies above the theoretical value predicted by (11), whereas for $N = 6, 10 \dots$ the error “notch” is deep and dips below the value predicted by (11). While the behavior at small values of α is of little practical value (due to the low efficiency and hence vulnerability to device mismatches), it is of considerable academic interest to be confronted with a simple circuit principle so clearly affording essentially perfect sinusoidal synthesis.

E. Effect of Component Tolerances

Practical accuracy will be influenced by nonideal transistor behavior (finite and current-dependent beta, emitter and base

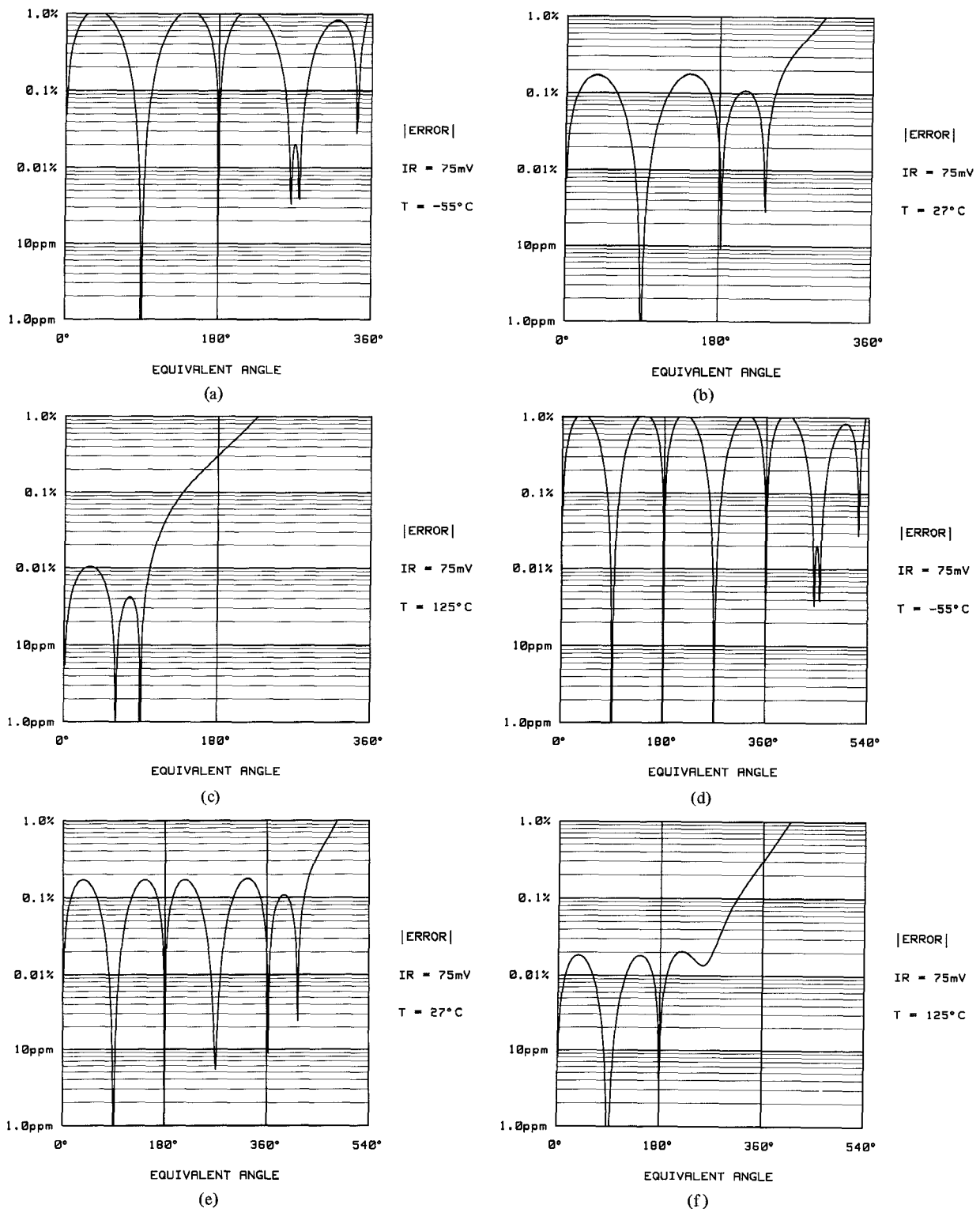


Fig. 7. Error-magnitude plots for -55°C , $+25^{\circ}\text{C}$, and $+125^{\circ}\text{C}$ (left to right) and the six- or eight-transistor circuit (top and bottom); $E_B = 75\text{ mV}$.

resistance, Early voltage, etc.), transistor mismatches (beta, V_{BE} , resistances), and tolerances in the current sources I and base resistors R . The interaction of these is sufficiently complex as to discourage a purely analytic approach, and recourse must be made to the use of some simple intuitive reasoning to delineate the obvious trouble spots, and to circuit simulation techniques to examine the consequences of realistic component tolerances.

The small voltages in the base network suggest immediately that V_{BE} mismatches will be a major source of error. At the zero crossings two adjacent transistors share most of I_E . If one device has a V_{BE} only $100\text{ }\mu\text{V}$ higher than the other, there is a net differential output of about $0.002I_E$ (at 300 K). Since the sine amplitude is typically $0.36I_E$, this represents an absolute error close to 0.5 percent. The need for very careful geometry control in these transistors is at once apparent. The

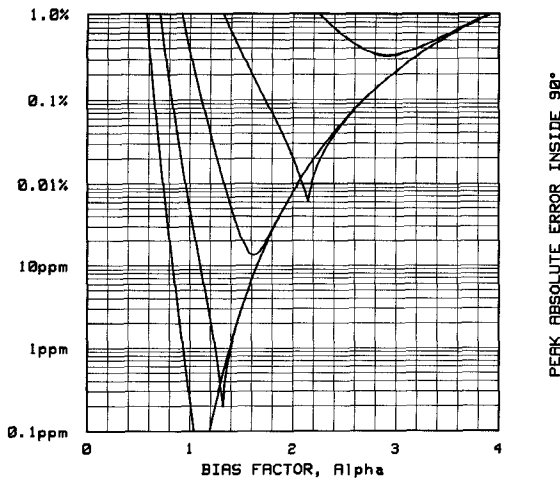


Fig. 8. Computed peak error inside $\pm 90^\circ$ for $N = 4, 6, 8, 10$, or 12 versus bias factor. Compare right-hand asymptote with the theoretical curve in Fig. 3.

same error will result when a temperature difference of only 0.05°C exists between adjacent devices, requiring similar care in the thermal layout of the chip. Indeed, these initial calculations would be quite discouraging were it not for the fact that production experience of several years with high-precision analog multipliers, in which very demanding matching requirements apply, prove that modern fabrication techniques can meet the challenge.

Nevertheless, prior to generating the first monolithic layout, an intensive investigation into the effects of component tolerances was undertaken, using a specially prepared simulation program for a desktop computer. Monte Carlo techniques were used to deal with the many variables, which included 1) tolerances in the current sources, I ; 2) tolerances in the base resistors, R ; 3) tolerances in V_{BE} ; 4) the effect of finite and current-dependent beta; 5) the effect of finite internal base resistance; 6) tolerances in base resistance; and 7) finite Early voltage. An adaptive curve-fitting algorithm was used to eliminate the absolute errors amenable to subsequent laser trimming during manufacture, namely, angular scaling, angular offset, amplitude scaling, and amplitude offset.

The results showed that typical manufacturing tolerances could be accepted with good yields to accuracies commensurate with those afforded by the sine-synthesis technique itself. An interesting discovery was that finite beta and base resistance can actually *lower* the approximation error under certain circumstances, and the operating bias levels and transistor geometries were accordingly optimized to take advantage of this fact. Also, these simulations (which were for a six-transistor circuit with $I = 150\ \mu\text{A}$, $R = 500\ \Omega$) optimized the minimax error, for each combination of tolerances, in the angular range -180° to $+180^\circ$. In practice, final trimming of the circuit for operation from -90° to $+90^\circ$, which represents a widespread application for the device, can consistently yield much lower errors.

F. An Alternative Implementation

The base network using equal resistors and current sources to generate the "rolling parabola" voltage distribution, which is a key concept to the implementation of this sine-synthesis

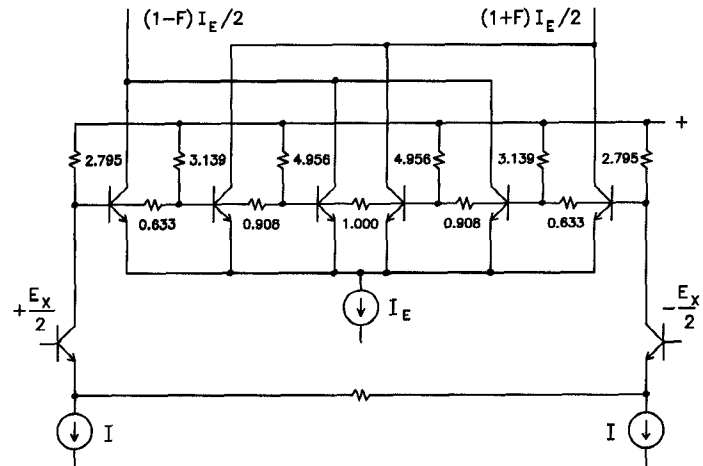


Fig. 9. An alternative network design using a tapered ladder network, with a suggested driver stage.

method, has the advantages of being canonic and easily analyzed and designed. An alternative network is possible using *only resistors*; it can be designed to be driven from angular inputs in the form either of voltage sources or current sources.

The basic idea is that *left-right symmetrical* ladder networks can be found such that the voltage distribution along the nodes decays parabolically from the driven end to the undriven end [14]. Thus, by superposition of *complementary* drive inputs, one at each end of the network, the combined parabolas form a distribution having a constant gradient and a linearly-positionable minimum or maximum (as in the network discussed earlier).

The most convenient arrangement is shown in Fig. 9, which also shows suitable resistor values in normalized form. A simple differential-voltage-to-differential-current converter provides a high-impedance angle-input interface. The effective bias voltage (E_B) is now proportional to the bias currents I . A potential advantage of this approach is that by using a translinear multiplier cell in place of the V - I converter, the current I can be PTAT, while the modulation index can be temperature stable. Thus, the distortion and efficiency can be held constant over temperature, and the network is attractive in simple sine-cosine synthesis since a second network for temperature stabilization is no longer required.

On the other hand, it is difficult to manufacture the irrational resistor ratios to high accuracy, and the multiplier cell would also introduce additional errors. On balance, this alternative is not very attractive at the present time, but its unique properties are deserving of further attention. Note that all of the theory and resulting characteristics derived for the regular network still apply, using simple transformations to rescale the angular input.

IV. MONOLITHIC IMPLEMENTATION

The monolithic circuit was developed with the objective of bringing together in one complete, readily understood microsystem the means to generate all the trigonometric functions, their extensions and their inverses, having either algebraic sign, externally-controlled or preset amplitude, low error, and a bandwidth of at least 1 MHz. Other objectives were to pro-

vide operation from supplies of ± 4.5 V to ± 18 V over temperatures from -55°C to $+125^\circ\text{C}$, load driving to at least ± 10 V into a $1\text{ k}\Omega$ load, signal-gating facilities (for pulsed-*CW* sine wave operation), and dynamic warning of improper input combinations (error trapping).

The prototype circuit uses a standard junction-isolated process with laser-trimmed thin-film resistors and is packaged in a 14-pin DIP. Functions are programmed by simple pin strapping and no external components are needed for the majority of applications. The sine networks use six transistors, providing accurate operation to $\pm 180^\circ$ (with a useful range to $\pm 360^\circ$) in the sine mode. Fig. 10 is a photomicrograph of the prototype IC.

To provide greater versatility, the production circuit will use a 16-pin package; one of the extra pins accesses the differential-input capability of the amplitude-control input, and the other is used to access (and optionally disable) the error-trapping system and incidentally permit fast gating of the output. Also, eight transistors are now used in the X network, to improve the sine/cosine accuracy at $\pm 360^\circ$ and extend the useful range to $\pm 540^\circ$.

In addition to the linear amplitude-control inputs the circuit provides precalibrated digitally selectable amplitudes of 1 V or 10 V. The bandgap reference circuit provides a stable, loadable output of $+1.800$ V for use primarily in setting up angular inputs of 90° . Fig. 11 shows the main elements of the final design.

During manufacture, laser trimming is used to calibrate angular scaling, the preset amplitudes, the linear-amplitude gain, and the reference output. It is also used to null the angular offset on both X and Y networks and other internal offsets.

After calibration the device exhibits the transfer characteristic

$$V_{\text{out}} = G_0 \left\{ (A_0 + A_1 - A_2) \frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} - (Z_1 - Z_2) \right\} \quad (14)$$

where

- G_0 is the open-loop gain of the output op amp, and can be considered infinite for most purposes;
- A_0 is the preset amplitude (0, 1 V, or 10 V);
- A_1 and A_2 are the external amplitude-control inputs;
- x_1, x_2, y_1 , and y_2 are the angles equivalent to voltage inputs $X1, X2, Y1$, and $Y2$, scaled 20 mV per degree; and
- $Z1$ and $Z2$ are the feedback and inverse-function inputs.

Note that the net amplitude

$$A = A_0 + A_1 - A_2 \quad (15)$$

must be greater than zero; however, if A_0 is enabled the input $A_1 - A_2$ can attain ± 1 V or ± 10 V and thus be used for *ac modulation* purposes in triwave-to-sine wave applications. For the standard functions $Z1$ is connected to V_{out} , closing the feedback around the output op amp when

$$V_{\text{out}} = A \frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} + Z2. \quad (16)$$

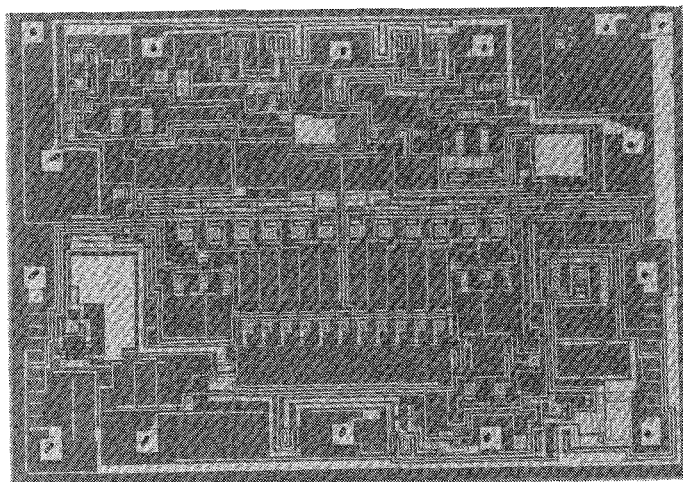


Fig. 10. Photomicrograph of the prototype chip. The two sine networks are at the center. Note extensive use of integral resistance units for tight matching.

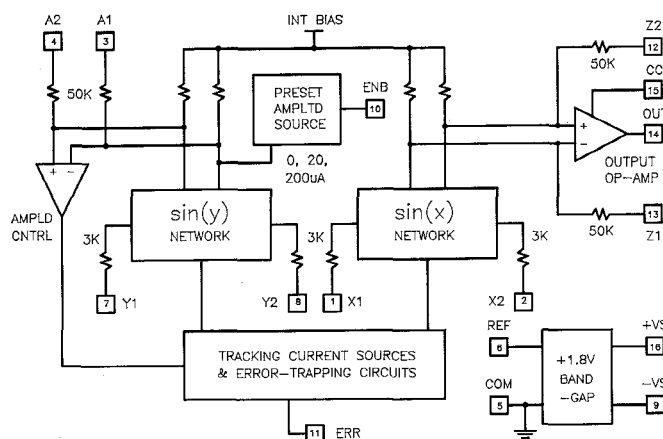


Fig. 11. Block schematic of the final version of the IC.

The desired function is then easily programmed using the identities shown in Table I. $Z2$ may be grounded or used as a summing input for generation of the offset functions, for example, $A \text{vers}(z) = A(1 - \sin(z)) = A \sin(-z) + A$, or the addition of the outputs of two or more devices, for example, in synthesizing $A \sin(a) + B \cos(b)$.

For inverse function generation, $Z1$ and $Z2$ are used as the main input, and V_{out} is fed back to the appropriate angle input/s. For example, to generate the arcsine, the device would first be set up for $-A \sin(u)$, where u is the angle corresponding to V_{out} . Applying (14) and noting that the operational amplifier forces the contents of the outer brackets to zero,

$$-A \sin(u) - (Z1 - Z2) = 0$$

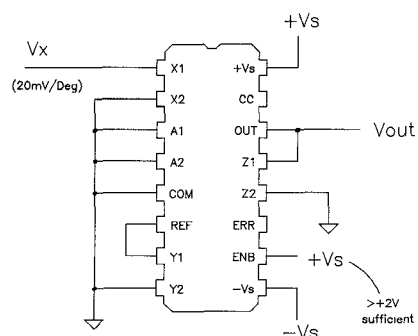
so

$$u = \arcsin \left\{ \frac{Z2 - Z1}{A} \right\}. \quad (17)$$

Two minor practical problems arise in the inverse modes. First, since the inverse functions are multivalued, some means must be provided to limit the equivalent angle to the principal

TABLE II
TYPICAL CHARACTERISTICS AT $\pm 15\text{ V}$, 25°C

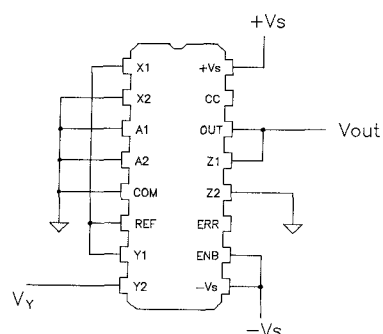
Angle Inputs X, Y		Main Output ($R_L \leq 1\text{ k}\Omega$)	
Resistance	$3.7\text{ k}\Omega$	Voltage swing	$\pm 13\text{ V}$
Scaling	$20\text{ mV}/^\circ \pm 0.2\%$	Offset ($A = 0$)	$\pm 5\text{ mV}$
Offset	$\pm 0.5^\circ$	Bandwidth (Sine mode, $A=1\text{ V}$)	1.5 MHz
Range		(Sine mode, $A=10\text{ V}$)	500 KHz
(X)	$\pm 540^\circ$	Law Conformance	
(Y)	0° to 180°	Sine (-90° to $+90^\circ$)	$\pm 0.02\%$
		(-180° to $+180^\circ$)	$\pm 0.2\%$
Amplitude Inputs A, Z		Cosine (-180° to $+180^\circ$)	$\pm 0.5\%$
Resistance	$50\text{ k}\Omega$	Tangent (-80° to $+80^\circ$)	$\pm 1\%$
Scaling	$1.00 \pm 0.2\%$	Power Requirements	
Linearity (0 to $+10\text{ V}$)	$\pm 0.2\%$	$\pm V_s$	4.5 V to 18 V
Reference Output	$1.800\text{ V} \pm 1\text{ mV}$	Quiescent current	4.5 mA

Basic 10V Sine Mode

$$V_{out} = 10\text{ V} \frac{\sin(X-0)}{\sin(90-0)} = 10\sin(X)$$

Useful range is $500^\circ < X < 500^\circ$

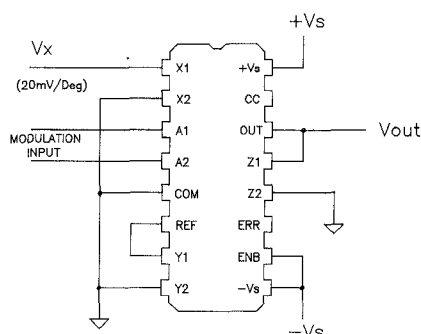
(a)

1V Secant Mode

$$V_{out} = 1\text{ V} \frac{\sin(90-0)}{\sin(90-Y)} = \frac{1}{\cos Y} = \sec Y \quad (=11.47\text{ V at } Q=85^\circ)$$

Principal range is $-90^\circ < Q < 90^\circ$

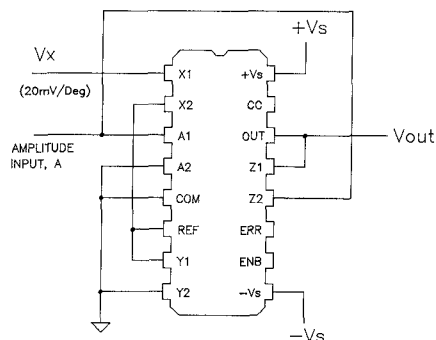
(d)

Sine Modulation Mode, 1V Carrier

$$V_{out} = (1V + A1 - A2) \frac{\sin(X-0)}{\sin(90-0)} = (1+A)\sin(X)$$

where $A = (A1 - A2) = \pm 1\text{ V max}$

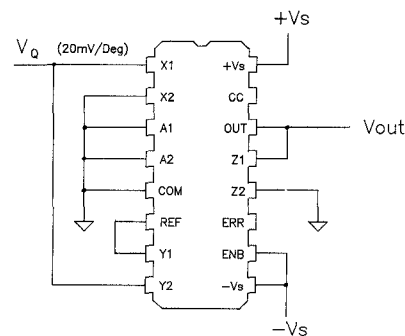
(b)

Versine (or Haversine) Mode

$$V_{out} = A \frac{\sin(X-90)}{\sin(90-0)} + A = A(-\cos(x)+1) = A \text{ vers}(x)$$

(Haversine is simply half the amplitude)

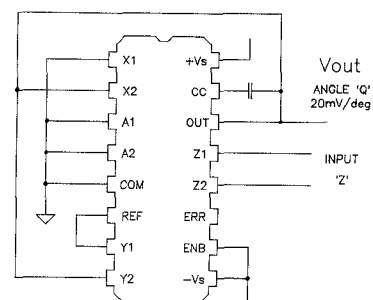
(e)

1V Tangent Mode

$$V_{out} = 1\text{ V} \frac{\sin(Q-0)}{\sin(90-Q)} = \frac{\sin Q}{\cos Q} = \tan Q \quad (=11.43\text{ V at } Q=85^\circ)$$

Principal range is $-90^\circ < Q < 90^\circ$

(c)

The 1V Arctangent Mode

$$V_{out} = G \left[(1\text{ V}) \frac{\sin(0-Q)}{\sin(90-Q)} - (Z1-Z2) \right]$$

The high op-amp gain G forces contents inside brackets to zero; hence

$$(1\text{ V})(-\tan Q) = (Z1-Z2)$$

and therefore

$$Q = \arctan (Z2-Z1)$$

[where Z is in volts]

(f)

Fig. 12. Six of the innumerable programming connections showing the ease of setting up a given function.

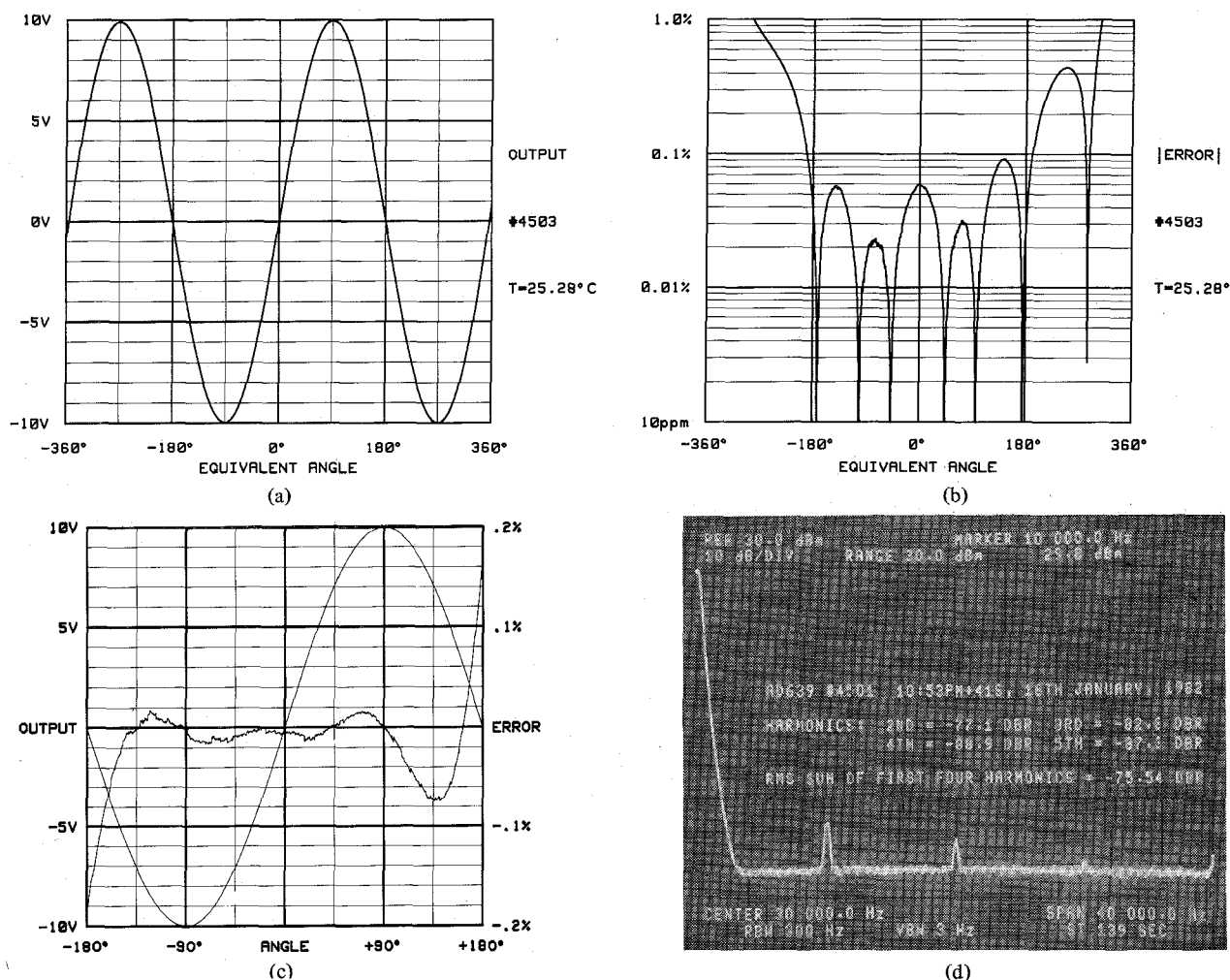


Fig. 1. Performance in the sine mode: (a) output; (b) log-magnitude of error calculated from (a) data; (c) device scaling adjusted very slightly, showing reduced error; (d) spectrum at 10 kHz.

range (in this example $\pm 90^\circ$). Now, the angle inputs are resistive, and V_{out} is limited by the op amp and supply voltages to reasonably well-defined values, so a resistor in the feedback path will suffice. More exact clamping to ± 1.8 V can be provided using external active circuitry. Where the principal range is not centered on zero (as is the case, for example, with the cosecant) a diode can be inserted in series with the connection to V_{out} .

Second, the loop gain in the inverse modes exceeds the value for which the output op amp is stable using only its internal compensation capacitor. Thus, access is provided to the appropriate node allowing the user to add an external stabilization capacitor.

Table II summarizes the major characteristics of the monolithic circuit and Fig. 12 shows just six of the innumerable programming configurations of which it is capable. Note that even when using the minimum supply voltages (nominally ± 5 V) the angular inputs can still be driven to $\pm 360^\circ$ (or ± 7.2 V) due to the use of thin-film resistive attenuators between the networks and the input nodes, which raise the internal network scaling of about 3 mV/° to the interface sensitivity of 20 mV/°.

V. PERFORMANCE

Full characterization of a monolithic nonlinear analog circuit of this functional complexity is a challenge in itself. The results presented here are condensed from data still being collected from measurements on the monolithic prototype, and serve to demonstrate that the main objectives have been met. The revised design, apart from extending the angular range of the X network and providing more versatility, also addresses a high-temperature limitation in the current part due to a design error which causes the devices in the shaping networks to saturate above 100°C .

A. Sine Mode

Using the basic sine-mode connections shown in Fig. 12(a) with the amplitude set to 10 V, the output can be measured on a point-by-point basis using a precision voltage source and a DVM. Fig. 13(a) shows typical results using a Data Precision 8200 calibrator, an HP3456A multimeter, an HP9845B computer for control and analysis, and drawn on a HP9872B plotter. This measurement system is used extensively to evaluate the devices and offers higher accuracy and resolution

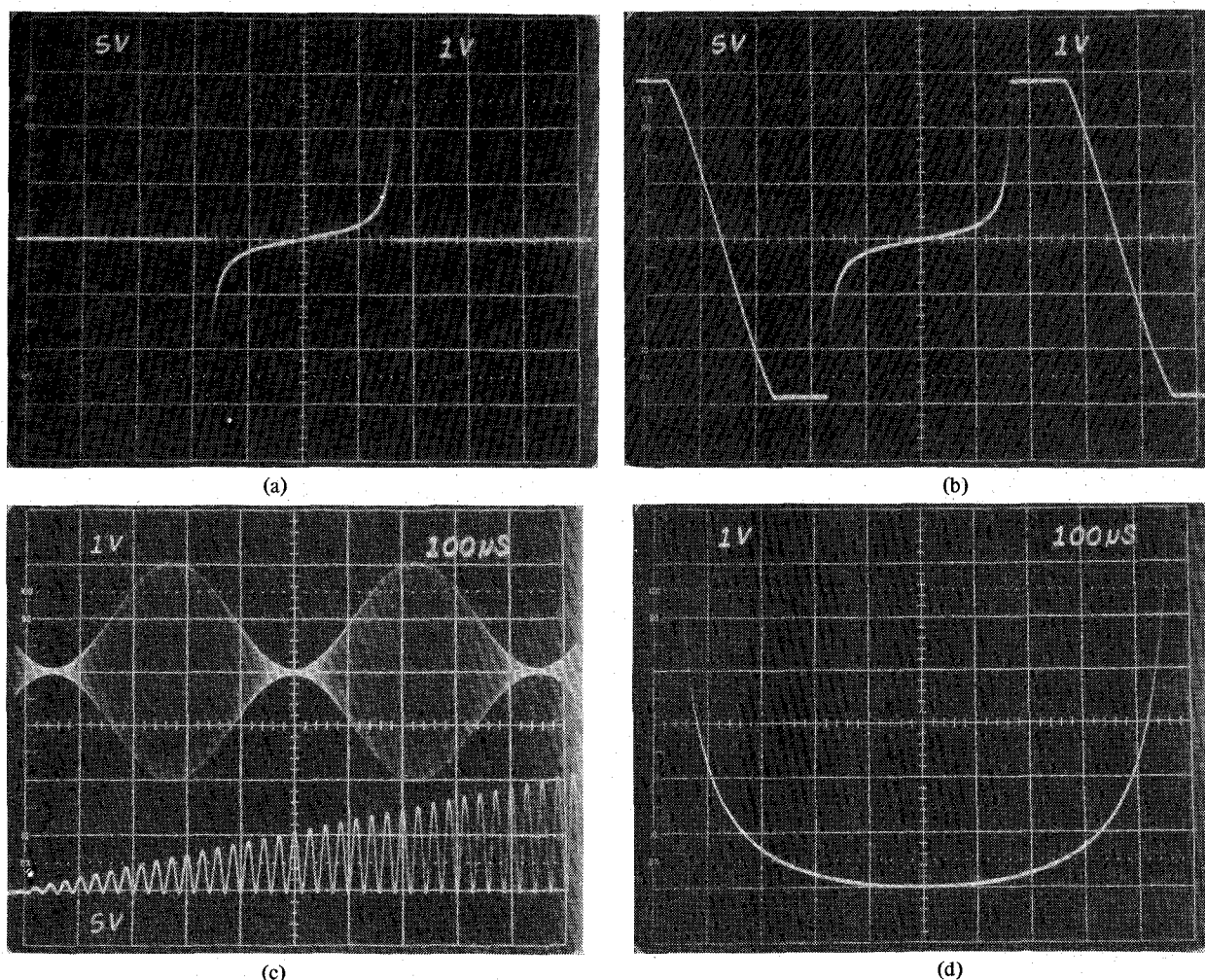


Fig. 14. (a) Tangent mode, with error trapping; (b) error trapping disabled; (c) sine-modulation modes; (d) secant mode.

than an oscilloscope plus the capability of computing errors using an ideal reference function. Fig. 13(b) shows the log magnitude of the *absolute* error (from all sources, including angular scaling, angular offset, amplitude scaling, and amplitude offset) for a typical part. The manufacturing trim algorithm minimizes the error over the central $\pm 180^\circ$, and it is seen to be under 0.1 percent. With a slight external adjustment the error over the central $\pm 90^\circ$ (the range usually of interest) can be reduced to less than 0.02 percent, as Fig. 13(c) shows, using a more conventional linear presentation; this is at the expense of error at $\pm 180^\circ$, now up to 0.18 percent. Fig. 13(d) shows the resulting spectrum at a fundamental frequency of 10 kHz; the largest harmonic is the second, at -77 dBr. The distortion increases with frequency, and typically measures -60 dBr at 100 kHz. Very careful adjustment of the triwave (generated here by an HP3325A function generator) is mandatory to achieve this spectral purity. Even an ideal sine shaper is vulnerable to variations in the amplitude, offset, linearity, and time symmetry of the driving waveform, and a significant proportion of the residual error can be attributed to such nonidealities in this case.

The -3 dB bandwidth of the integrated-circuit output stage

is 1.5 MHz; the slew rate of 40 V/ μ s provides a full-power (± 10 V) bandwidth of at least 500 KHz. Using an external high-speed op amp driven directly from the sine-shaping network, the large-signal bandwidth can be extended to 5 MHz.

An interesting possibility opened up by the large angular range is that of implementing a frequency tripler, using a triwave input of ± 5.4 V which corresponds to an angular input of $\pm 270^\circ$. Now, each cycle of the triwave generates three sinewave cycles. Measurements show the largest residue (subharmonic or harmonic) is typically -62 dBr at ± 10 V output and an output frequency of 50 kHz.

B. Other Modes

Operation in all other modes has been verified and the accuracy in the tangent and arctangent mode has been characterized using the computer-controlled data acquisition system. Fig. 14(a) shows the tangent at an amplitude of 1 V and with the error-trapping feature operational [connections of Fig. 12(c)]. The angular input is shown on the horizontal axis; cutoff occurs for inputs greater than 1.65 V, corresponding to $\pm 82.5^\circ$. The "ERR" pin generates a flag output easily interfaced with a variety of external devices. The error trap is

disabled by connecting this pin to $-V_S$; Fig. 14(b) shows that the output is incorrect when the angular input is in the wrong range. The "ERR" pin can also be used to rapidly gate the output, which is particularly useful in the sine wave mode; the switching threshold is at +1.5 V and compatible with most logic families.

Fig. 14(c) shows the use of sine-modulation modes. In the upper trace, the connections of Fig. 12(b) are used, with a ± 1 V modulation input the "carrier" frequency is 300 kHz. In the lower trace, the versine mode was used [Fig. 12(e)]. Finally, Fig. 14(d) shows the operation in the 1 V secant mode, for $\pm 90^\circ$ [Fig. 12(d)]; predictably, the output is +1 V at zero angle, +1.7 V at $\pm 54^\circ$, +3.24 V at $\pm 72^\circ$, etc. The cosecant and cotangent modes behave with similar predictability.

VI. CONCLUSION

A monolithic laser-trimmed analog microsystem has been developed which provides accurate synthesis of all trigonometric functions and their inverses in an easily programmed 16-pin package, based on a novel circuit architecture and high-precision sine-shaping network described in this paper. The bandwidth is limited by the output amplifier to 1.5 MHz, but could in the future be extended to 5 MHz by providing direct access to the current-mode outputs and using an external amplifier. This circuit expands the growing family of fully calibrated analog computational integrated circuits and offers a low-cost alternative to digital implementations where simplicity and speed are primary considerations.

APPENDIX I

ANALYSIS OF THE GENERAL SINE NETWORK

The general network comprises N identical, isothermal, and ideal transistors, $N-1$ identical resistors and $N-2$ identical current sources, where $N \geq 4$ and assumed here to be even, resulting in an overall function having odd-order symmetry. The differential voltage E_x determines the instantaneous *angle* of the function; the current I_E determines its *magnitude*.

The voltage at each base node results from the superposition of a "fixed" component due to the currents I flowing in the base resistors and a "variable" component due to the linear division of E_x as follows:

$$V_{Bn} = (n-1) \left\{ \frac{(N-n)IR}{2} + \frac{E_x}{N-1} \right\}. \quad (\text{A.1})$$

The locus of this array of voltages forms a parabola, the apex of which is centered when $E_x = 0$, and moves to the left or right as E_x is increased or decreased, respectively. I_E is steered mainly into the (n-p-n) transistor whose base is most positive, the acuity of switching being dependent on the bias factor

$$\alpha = \frac{IR}{kT/q} = \frac{E_B}{kT/q}. \quad (\text{A.2})$$

For a locally-symmetric voltage distribution, the zero crossings of the output function occur whenever adjacent bases are at the same voltage

$$V_{Bn} = V_{B(n+1)}. \quad (\text{A.3})$$

Solving (A.1) and (A.2), E_x has the multiple values

$$E_x = (N-1) \left(\frac{N}{2} - n \right) E_B \quad (\text{A.4})$$

from which it is apparent that E_x must change by $(N-1)E_B$ to move from one zero-crossing to the next. The equivalent angle is therefore

$$x = \frac{\pi E_x}{(N-1)E_B}. \quad (\text{A.5})$$

Substituting for E_x in (A.1) yields

$$V_{Bn} = (n-1) \left\{ \frac{N-n}{2} + \frac{x}{\pi} \right\} E_B. \quad (\text{A.6})$$

The corresponding collector currents I_{Cn} can now be calculated as follows:

$$I_{Cn} = I_E \frac{\exp \frac{V_{Bn}}{kT/q}}{\sum_{n=1}^N \exp \frac{V_{Bn}}{kT/q}} \quad (\text{A.7})$$

and using (A.5) and (A.6) this becomes

$$I_{Cn} = I_E \frac{\exp \left[\alpha(n-1) \left\{ \frac{N-n}{2} + \frac{x}{\pi} \right\} \right]}{\sum_{n=1}^N \exp \left[\alpha(n-1) \left\{ \frac{N-n}{2} + \frac{x}{\pi} \right\} \right]}. \quad (\text{A.8})$$

Finally, the *normalized* output is obtained by summing alternate collector currents in antiphase as follows:

$$\begin{aligned} F(x, \alpha, N) &= \frac{I_{\text{out}}}{I_E} \\ &= (-1)^{N/2} \frac{\sum_{n=1}^N (-1)^n \exp \left[\alpha(n-1) \left\{ \frac{N-n}{2} + \frac{x}{\pi} \right\} \right]}{\sum_{n=1}^N \exp \left[\alpha(n-1) \left\{ \frac{N-n}{2} + \frac{x}{\pi} \right\} \right]} \end{aligned} \quad (\text{A.9})$$

where the factor $(-1)^{N/2}$ accounts for the alternation in the effective phase of the function as pairs of devices are added to the network.

This expression provides little insight, but numerical evaluation soon proves the close similarity between this function and the sine over angular ranges up to $\pm(N-2)\pi/2$ radians. Using a method suggested by Genin [15] and developed by Boyle it has been shown that for $N \rightarrow \infty$ and small values of α

$$F(x, \alpha) \rightarrow \eta \sin x \text{ exactly} \quad (\text{A.10})$$

where η is the network efficiency

$$\eta = 2 \exp \left\{ -\frac{\pi^2}{2\alpha} \right\}. \quad (\text{A.11})$$

This agrees very closely with numerically calculated efficiency using (A.9), for $\alpha < 3.5$, above which value the distortion be-

comes excessive. The simple linear approximation

$$\eta = 0.214\alpha - 0.2568 \quad (\text{A.12})$$

is within 1 percent for the useful range of α from 2 to 3.5.

ACKNOWLEDGMENT

This work represents the culmination of many years of effort in searching for a satisfactory general method of trigonometric function synthesis using analog techniques. Along the way, many people provided valuable assistance. Special thanks to G. Boyle for his help in finding a rigorous proof of the convergence of the network function to an exact sine; to M. Libert for his excellent mask layouts; F. Mapplebeck for his laser trimming expertise; to M. Gerstenhaber, K. Weigel, and D. Whitney for their support during product development and evaluation; and to M. Cordrey for her patience and accuracy in preparing several revisions of this paper.

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